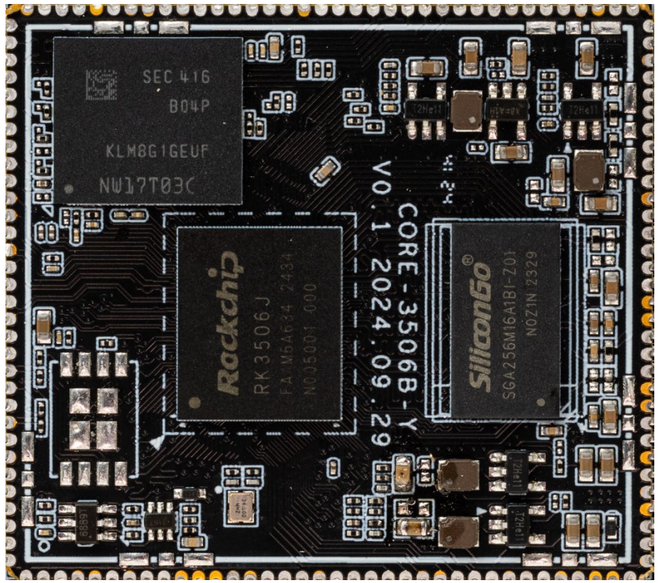
Quad-core Core Board

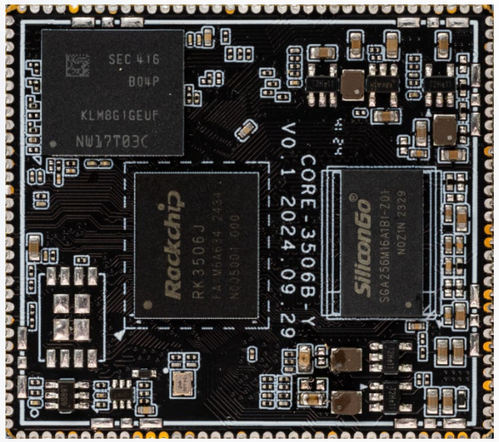
- Core-3506BY(Commercial)
- Core-3506JY(Industrial)



V0.1 2024-1-3

T-CHIP INTELLIGENCE TECHNOLOGY

Product features



The new industrial chip RK3506

It adopts Rockchip's new industrial chip RK3506 series, 22nm advanced process technology, integrated triple-core ARM Cortex-A7 + single-core Cortex-M0, the main frequency is up to 1.6GHz.

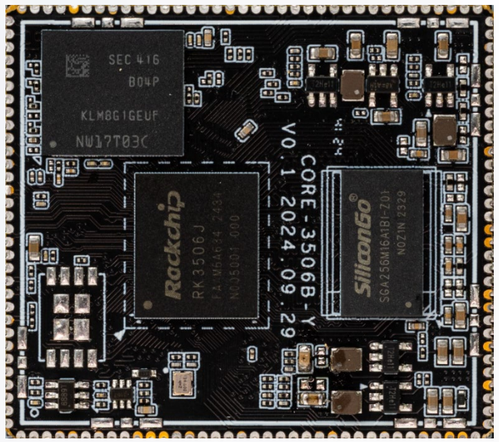
Low latency and high real-time performance

It supports AMP multi-core heterogeneous architecture, and one chip can support Linux, RTOS, and Bare-metal flexible combinations, such as 2×Cortex-A7 Linux + 1×Cortex-A7 RTOS + Cortex-M0 HAL or 3×Cortex-A7 RTOS + Cortex-M0 HAL and other combinations, using the standard RPMsg inter-core communication mechanism.

Stamp hole interface, small size and high performance

The stamp hole interface allows for optimal data transmission and expansion, and the compact size of the design saves more valuable space. It adopts high-quality components and stable operation, which can be applied to various industrial products.

Product features



Supports multiple operating systems

The SDK supports Linux Kernel 6.1, provides support based on Buildroot system, and supports AMP multi-core heterogeneous systems, and implements the RTOS SMP mode for the first time on the multi-core architecture of the Rockchip platform, and adds multi-core scheduling support in the real-time system.

Abundant industry-specific interfaces

It has a wealth of interfaces required for industrial gateways, including dual 100M Ethernet, 2 × CAN FD, DSMC parallel communication bus, 6 × UART, 12 × PWM, 3 × SPI, etc.

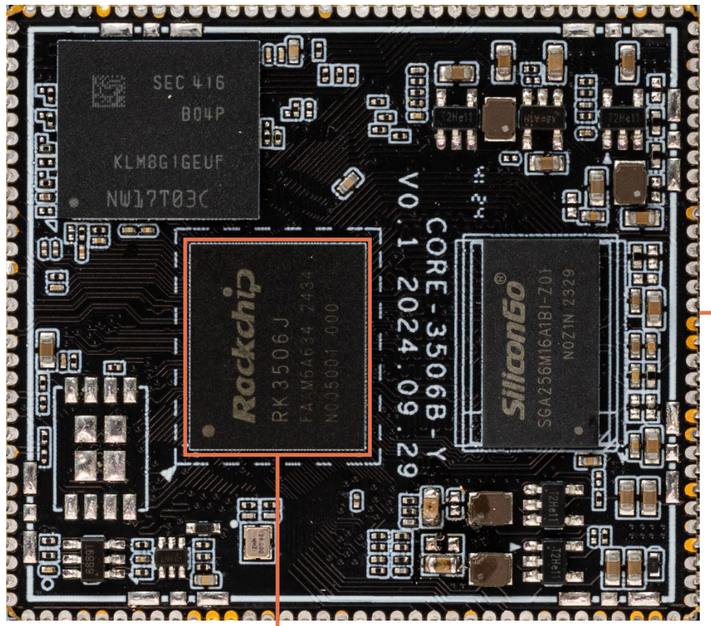
A wide range of applications

It is widely used in: industrial HMI, PLC, industrial gateway, industrial control, smart home, home appliance display control, handheld POS machine and other industries.

Specifications

		Core-3506BY (Commercial)	Core-3506JY (Industrial)
Basic Specifications	SOC	Rockchip RK3506B	Rockchip RK3506J
	CPU	Quad-core 32-bit processor (3×Cortex-A7+1×Cortex-M0), 22nm advanced process technology, main frequency up to 1.6GHz	Quad-core 32-bit processor (3×Cortex-A7+1×Cortex-M0), 22nm advanced process technology, normal mode main frequency up to 1.2GHz, overdrive mode main frequency up to 1.5GHz
	Image processing	Built-in 2D diagramming engine	
	Video decoding	Video Soft Solution: 720P@30fps, 480P@60fps H.264/MJPEG, support RTSP video streaming	
	RAM	512MB DDR3 (256MB/512MB optional)	
	Storage	8GB eMMC, 256MB SPI Flash (optional)	
	OS	Linux	
	Interface	Stamp hole (136Pin, 1.2mm pitch)	
	Power	5V (voltage tolerance ± 5%)	
	Power consumption	Max: 1.5W(5V/300mA) Normal: 1W(5V/200mA) Min(Sleep): Not supporting sleep mode	Max: 1.5W(5V/300mA) Normal: 1W(5V/200mA) Min(Sleep): 0.2W(5V/40mA)
	Size	45.0mm × 40.2mm × 3.2mm	
	Weight	≈7g	
	Environment	Operating Temperature: -20℃ ~ 60℃ Storage Humidity: 10% ~ 90%RH (non-condensing)	Operating Temperature: -40℃ ~ 85℃ Storage Humidity: 10% ~ 90%RH (non-condensing)
Interface Specifications	Internet	2 × RMII, support 10/100Mbps data transfer rate	
	Video input	Support DVP (Flexbus)	
	Video output	Supports parallel/serial MCU/RGB LCD interfaces: 24-bit (RGB888), 18-bit (RGB666), 16-bit (RGB565) Supports BT.656/BT.1120 Supports MIPI-DSI (2Lanes, 1.5Gbps/lane), maximum output resolution: 1280 ×1280@60fps	
	Audio	5 × SAI, 1 × ADC, 2 × DSM, 1 × I2S/TDM(2ch), 1 × I2S/PCM(1ch), 1 × PDM RX(8ch), 1 × SPDIF TX(8ch), 1 × SPDIF RX(8ch) Supports 3A: AEC (Echo Cancellation), ANR (Noise Suppression), AGC (Automatic Gain Control) Supports multi-MIC array processing: typically including beamforming, blind source separation, and source localization Support voice wake-up/detection: voice wake-up, keyword recognition, acoustic event detection, crying detection, glass shattering and beep detection	
	USB	2 × USB2.0 (OTG)	
	SAI	5 × SAI: SAI0 supports 1 TX lane and 4 RX lanes SAI1 supports 4 TX lanes and 1 RX lane SAI2/3 supports 1 TX lane and 1 RX lane SAI4 supports 1 RX lane Support I2S/TDM/PCM mode, support the highest sampling rate: 192KHz	
	PWM	12 × PWM	
	SPI	3 × SPI (Supports serial master and serial slave modes, software configurable)	
	I2C	3 × I2C (Supports 7-bit and 10-bit address modes, data rates up to 100kbps in standard mode, up to 400kbps in fast mode, and up to 1Mbps in fast mode Plus)	
	UART	6 × UART (Built-in 2-way 64 bits FIFO, TX and RX can be used respectively; Support 5-bit, 6-bit, 7-bit, 8-bit serial data transceiver and receiver, baud rate up to 4Mbps; All 6 UARTs support automatic flow control mode and RS485 mode)	
	CAN	2 × CAN FD	
	DSMC	DSMC double data rate serial interface: Supports up to 4 chips and supports 8-wire or 16-wire serial transmission mode	
	Flexbus	1 × Flexbus (Support 1, 2, 4, 8, 16 bit data parallel transmission, clock up to 100MHz)	
	Watchdog	External watchdog	
	Other interfaces	4 × SARADC, 1 × SDMMC, 93 × GPIO	

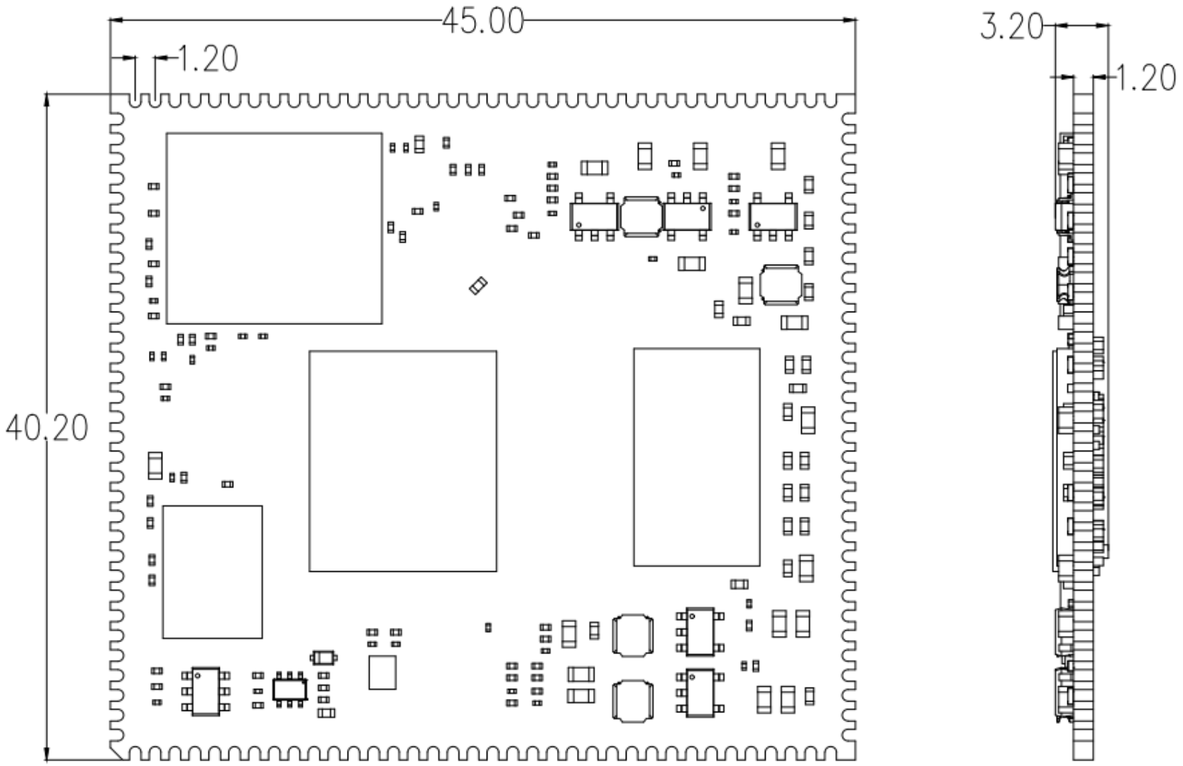
Core Board Interface description

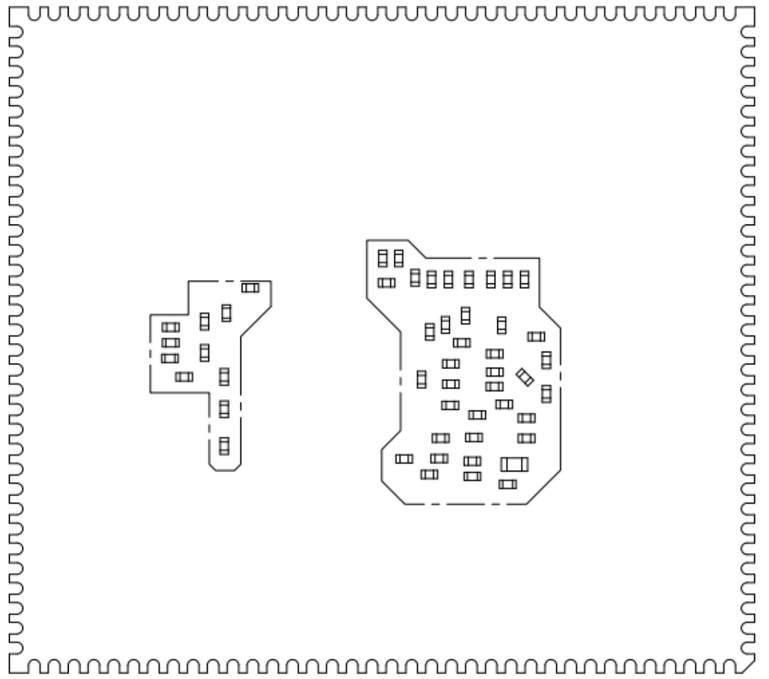


Stamp hole interface
136Pin, 1.2mm Pitch

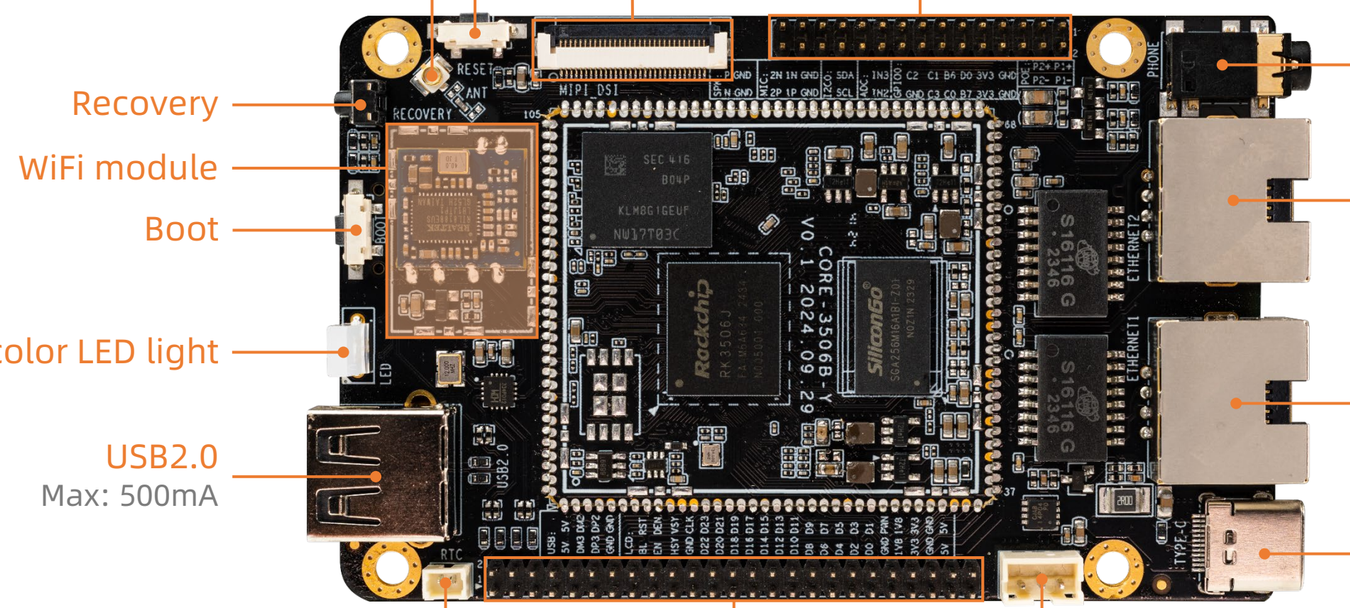
RK3506B/RK3506J
Main frequency up to 1.6GHz/1.2GHz

Core Board Dimension

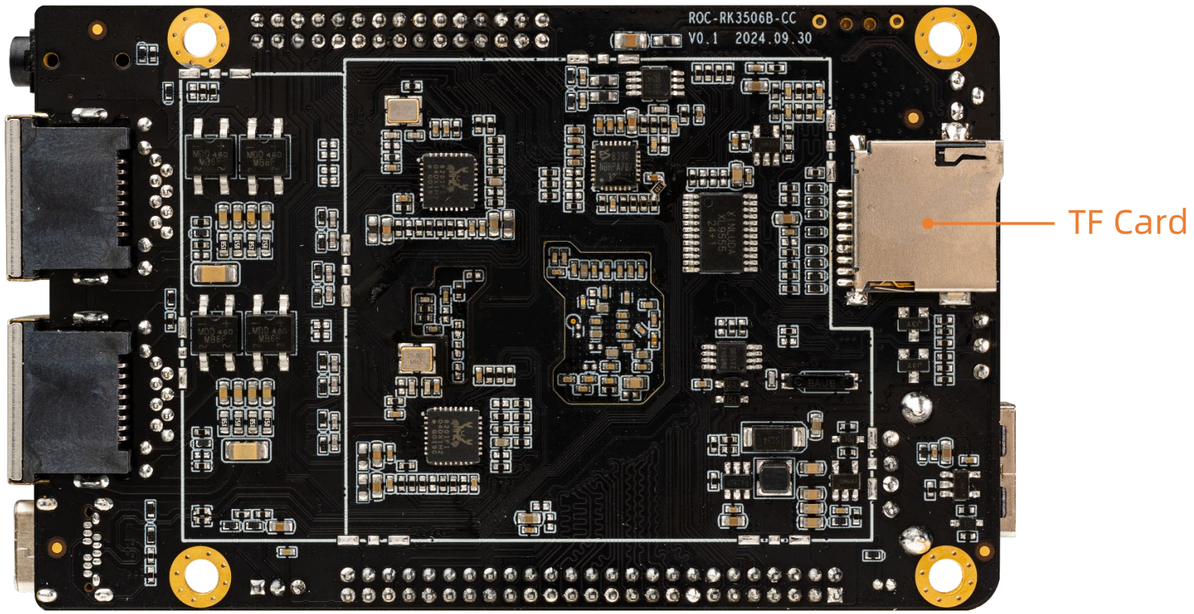




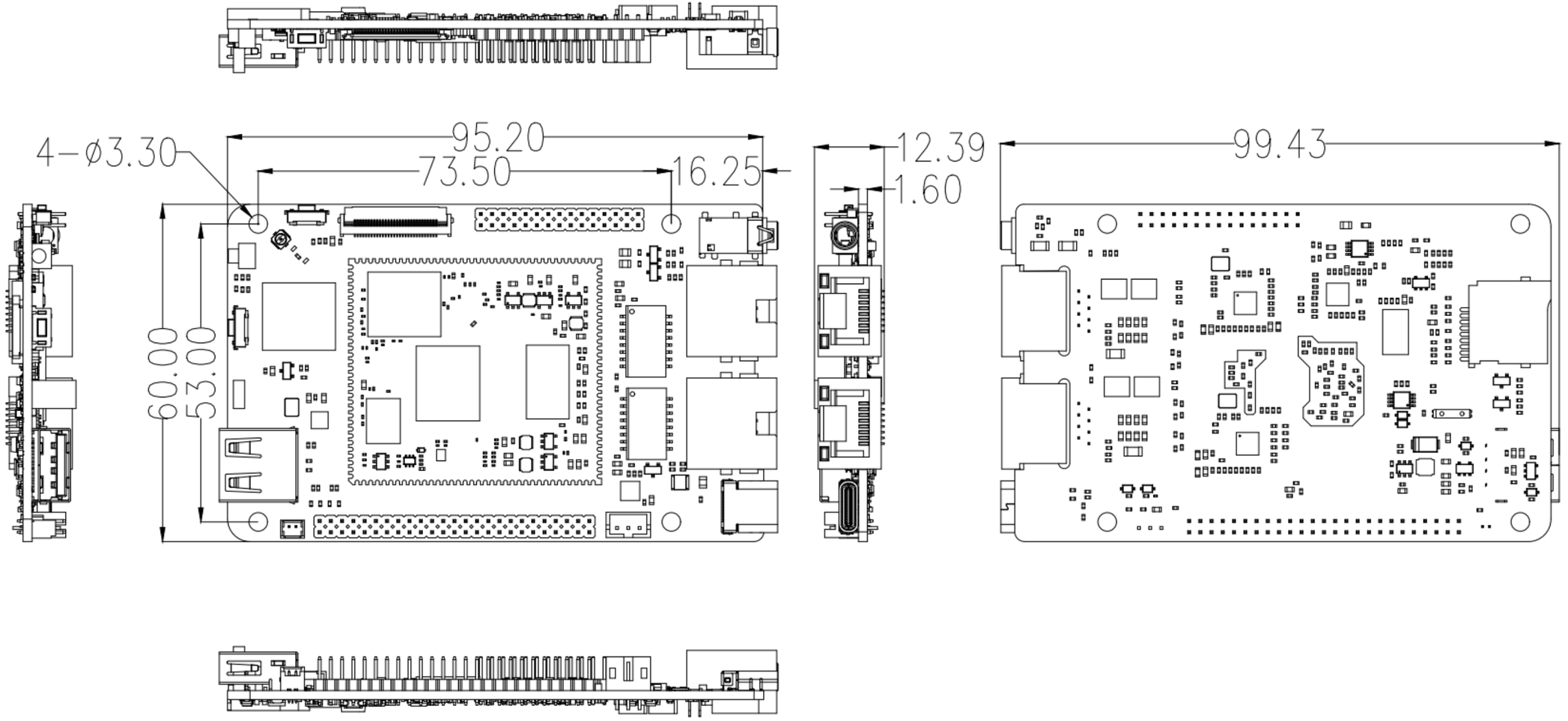
Mainboard Interface description



Mainboard Interface description



Mainboard Dimension



Interface definition

Notes1:
① : Pad types: I = input, O = output, I/O = input/output (bidirectional) , I/GPIO = When used as GPIO port, it is input (I) ,A = Analog , G= Ground , P = power supply , DOWN = Internal pull down , UP = Internal pull UP
0 = Lowe Level 1 = High level

Pin	CORE-3506B-Y pin definition	RK3506B Pin No.	Pad type	IO Power domain	IO Pull	Function for ROC-RK3506B-CC	Default function description
1	GND		G			GND	GND
2	VO_LCDC_D16/DSMC_INT3/FLEXBUS1_D11/FLEXBUS0_D14/FLEXBUS1_CSN_M1/SAI2_LRCK_M1/RM_IO26/GPIO1_B3_d	B5	I/O	3.3V	DOWN	LCD_D16	LCD_D16
3	VO_LCDC_D15/DSMC_D6/FLEXBUS1_D12/FLEXBUS0_D13/FLEXBUS0_CSN_M2/GPIO1_B4_d	1A1	I/O	3.3V	DOWN	LCD_D15	LCD_D15
4	VO_LCDC_D14/DSMC_D7/FLEXBUS1_D13/FLEXBUS0_D12/FLEXBUS1_CSN_M2/GPIO1_B5_d	C3	I/O	3.3V	DOWN	LCD_D14	LCD_D14
5	VO_LCDC_D13/DSMC_CSN0/FLEXBUS1_D14/FLEXBUS0_D11/FLEXBUS0_CSN_M3/GPIO1_B6_d	A3	I/O	3.3V	DOWN	LCD_D13	LCD_D13
6	VO_LCDC_D12/DSMC_RDYN/FLEXBUS1_D15/FLEXBUS0_D10/FLEXBUS1_CSN_M3/GPIO1_B7_d	B3	I/O	3.3V	DOWN	LCD_D12	LCD_D12
7	VO_LCDC_D11/DSMC_RESETN/FLEXBUS1_CLK/DSMC_INT1/FLEXBUS0_CSN_M4/DSMC_SLV_CLK/GPIO1_C0_d	A2	I/O	3.3V	DOWN	LCD_D11	LCD_D11
8	VO_LCDC_D10/DSMC_D8/FLEXBUS0_CLK/DSM_AUD_RN_M0/FLEXBUS1_CSN_M4/SAI2_MCLK_M1/DSMC_SLV_DQS0/GPIO1_C1_d	B2	I/O	3.3V	DOWN	LCD_D10	LCD_D10
9	VO_LCDC_D9/DSMC_D9/FLEXBUS0_D9/DSM_AUD_RP_M0/FLEXBUS0_CSN_M5/SAI2_SDI_M1/RM_IO27/DSMC_SLV_D0/GPIO1_C2_d	B1	I/O	3.3V	DOWN	LCD_D9	LCD_D9
10	VO_LCDC_D8/DSMC_D10/FLEXBUS0_D8/FLEXBUS1_CSN_M5/SAI2_SDO_M1/RM_IO28/DSMC_SLV_D1/GPIO1_C3_d	C2	I/O	3.3V	DOWN	LCD_D8	LCD_D8
11	VO_LCDC_D7/DSMC_D11/FLEXBUS0_D7/DSMC_SLV_D2/GPIO1_C4_d	C1	I/O	3.3V	DOWN	LCD_D7	LCD_D7
12	VO_LCDC_D6/DSMC_D12/FLEXBUS0_D6/DSMC_SLV_D3/GPIO1_C5_d	D3	I/O	3.3V	DOWN	LCD_D6	LCD_D6
13	VO_LCDC_D5/DSMC_D13/FLEXBUS0_D5/DSMC_SLV_D4/GPIO1_C6_d	E3	I/O	3.3V	DOWN	LCD_D5	LCD_D5
14	VO_LCDC_D4/DSMC_D14/FLEXBUS0_D4/DSMC_SLV_D5/GPIO1_C7_d	E2	GND	3.3V	DOWN	LCD_D4	LCD_D4

Interface definition

15	VO_LCDC_D3/DSMC_D15/FLEXBUS0_D3/DSM_AUD_LN_M0/DSMC_SLV_D6/GPIO1_D0_d	**E1**	I/O	3.3V	DOWN	LCD_D3	LCD_D3
16	VO_LCDC_D2/DSMC_DQS1/FLEXBUS0_D2/DSM_AUD_LP_M0/UART5_RTSN_M1/RM_IO29/DSMC_SLV_D7/GPIO1_D1_d	**F3**	I/O	3.3V	DOWN	LCD_D2	LCD_D2
17	VO_LCDC_D1/DSMC_CSN2/FLEXBUS0_D1/UART5_TX_M1/RM_IO30/DSMC_SLV_CSN0/GPIO1_D2_d	**F2**	I/O	3.3V	DOWN	LCD_D1	LCD_D1
18	VO_LCDC_D0/DSMC_CSN3/FLEXBUS0_D0/UART5_RX_M1/RM_IO31/DSMC_SLV_RDYN/GPIO1_D3_d	**G3**	I/O	3.3V	DOWN	LCD_D0	LCD_D0
19	GND					GND	
20	VCC_IO_1（GPIO1 power Inuput,default NC)		P	1.8V/3.3V		NC	NC (GPIO1 power input，default NC)
21	OSC_CLK_OUT/REF_CLK0_OUT/GPIO0_D0_d	**G1**	I/O	1.8V	DOWN	GPIO0_D0_d	HP_DET, Active H
22	UART0_RX/JTAG_TMS_M1/RM_IO23/GPIO0_C7_u	**J1**	I/O	3.3V	UP	UART0_RX	UART0_RX Debug
23	UART0_TX/JTAG_TCK_M1/RM_IO22/GPIO0_C6_u	**J2**	I/O	3.3V	UP	UART0_TX	UART0_TX Debug
24	ETH_CLK0_25M_OUT/AUPLL_CLK_IN/RM_IO20/GPIO0_C4_d	**K2**	I/O	3.3V	DOWN	GPIO0_C4_d	RXER/FXEN1
25	REF_CLK1_OUT/SPI0_MISO/RM_IO18/GPIO0_C2_d	**L1**	I/O	3.3V	DOWN	GPIO0_C2_d	GPIO0_C2_d To J6
26	ETH_CLK1_25M_OUT/SPI0_CSN0/RM_IO19/GPIO0_C3_d	**L2**	I/O	3.3V	DOWN	GPIO0_C3_d	GPIO0_C3_d To J6
27	SPI0_MOSI/RM_IO17/GPIO0_C1_d	**M3**	I/O	3.3V	DOWN	GPIO0_C1_d	GPIO0_C1_d To J6
28	SPI0_CLK/RM_IO16/GPIO0_C0_d	**M2**	I/O	3.3V	DOWN	GPIO0_C0_d	GPIO0_C0_d To J6
29	SAI1_SDO2/SPI1_CSN0/RM_IO14/GPIO0_B6_d	**N3**	I/O	3.3V	DOWN	GPIO0_B6_d	GPIO0_B6_d To J6/(TP_INT)
30	SAI1_SDO1/RM_IO13/GPIO0_B5_d	**N1**	I/O	3.3V	DOWN	GPIO0_B5_d	RXER/FXEN0
31	SAI1_SDO3/SPI0_CSN1/RM_IO15/GPIO0_B7_d	**N2**	I/O	3.3V	DOWN	GPIO0_B7_d	GPIO0_B7_d To J6
32	SAI1_SDO0/RM_IO12/GPIO0_B4_d	**P3**	I/O	3.3V	DOWN	SAI1_SDO0	SAI1_SDO0

Interface definition

33	SAI1_SDI/RM_IO11/GPIO0_B3_d	**P2**	I/O	3.3V	DOWN	SAI1_SDI	SAI1_SDI
34	SAI1_LRCK/SPI1_MISO/RM_IO10/GPIO0_B2_d	**R3**	I/O	3.3V	DOWN	SAI1_LRCK	SAI1_LRCK
35	SAI1_SCLK/SPI1_MOSI/RM_IO9/GPIO0_B1_d	**R1**	I/O	3.3V	DOWN	SAI1_SCLK	SAI1_SCLK
36	SAI1_MCLK/SPI1_CLK/RM_IO8/GPIO0_B0_d	**R2**	I/O	3.3V	DOWN	SAI1_MCLK	SAI1_MCLK
37	VCC5V0_SYS		P	5.0V		**VCC5V0_SYS**	System Power supply INPUT Input Voltag :5.0V,+/-5% Input current: Type 200mA ;Max 300mA
38	VCC5V0_SYS		P	5.0V			
39	VCC5V0_SYS		P	5.0V			
40	VCC5V0_SYS		P	5.0V			
41	VCC5V0_SYS		P	5.0V			
42	VCC5V0_SYS		P	5.0V			
43	GND		G			GND	GND
44	GND		G				
45	GND		G				
46	GND		G				
47	GND		G				
48	GND		G				
49	GND		G				
50	NPOR	**T3**	I/O	3.3V	UP	System Reset Input	Active L

Interface definition

51	SAI0_SDI3/SPI1_CSN1/RM_IO7/GPIO0_A7_d	**T2**	I/O	3.3V	DOWN	GPIO0_A7_d	RTC_INT Input,Active L
52	SAI0_SDI2/RM_IO6/GPIO0_A6_d	**U3**	I/O	3.3V	DOWN	GPIO0_A6_d	TP_INT Iput,Active L
53	SAI0_SDI1/RM_IO5/GPIO0_A5_d	**U1**	I/O	3.3V	DOWN	I2C0_SDA	I2C0_SDA Core board pull up Resistor 2.2K
54	SAI0_SDI0/RM_IO4/GPIO0_A4_d	**U2**	I/O	3.3V	DOWN	I2C0_SCL	I2C0_SCL Core board pull up Resistor 2.2K
55	GND		G			GND	GND
56	SAI0_SDO/RM_IO3/GPIO0_A3_d	**V2**	I/O	3.3V	DOWN	GPIO0_A3_d	BL_PWM
57	GND		G			GND	GND
58	GND		G			GND	GND
59	GND		G			GND	GND
60	VCC_IO_4（GPIO4 power Inuput,default NC)		P	1.8/3.3V		NC	NC (GPIO4 power input，default NC)
61	VCC_1V8（OUTPUT)		P			1.8V Output, Max 100mA	1.8V Output, Max 100mA
62	VCC_1V8（OUTPUT)		P				
63	VCC_IO_3（GPIO3 power Inuput,default NC)		P	1.8/3.3V		NC	NC (GPIO3 power input，default NC)
64	VCC_3V3（OUTPUT)		P	GND		3.3V Output, MAX 500mA	3.3V Output, MAX 500mA
65	VCC_3V3（OUTPUT)		P				
66	GND		G			GND	GND
67	UART5_RTSN_M0/ETH_RMII1_MDIO/GPIO3_B5_d	**P21**	I/O	3.3V	DOWN	RMII1_MDIO	RMII1_MDIO
68	UART5_TX_M0/ETH_RMII1_MDC/GPIO3_B4_d	**P23**	I/O	3.3V	DOWN	RMII1_MDC	RMII1_MDC

Interface definition

69	UART5_RX_M0/ETH_RMII1_TXEN/GPIO3_B3_d	**P22**	I/O	3.3V	DOWN	RMII1_TXEN	RMII1_TXEN
70	UART5_CTSN_M0/ETH_RMII1_TXD1/GPIO3_B2_d	**N21**	I/O	3.3V	DOWN	RMII1_TXD1	RMII1_TXD1 (core board series Resistor 22R)
71	SAI2_LRCK_M0/ETH_RMII1_TXD0/GPIO3_B1_d	**M21**	I/O	3.3V	DOWN	RMII1_TXD0	RMII1_TXD0 (core board series Resistor 22R)
72	GND		G			GND	GND
73	SAI2_SDO_M0/ETH_RMII1_CLK/GPIO3_B0_d	**M23**	I/O	3.3V	DOWN	RMII1_CLK	RMII1_CLK (core board series Resistor 22R)
74	SAI2_MCLK_M0/ETH_RMII1_RXDVCRS/GPIO3_B6_d	**R22**	I/O	3.3V	DOWN	RMII1_RXDV_CRS	RMII1_RXDV_CRS
75	SAI2_SCLK_M0/ETH_RMII1_RXD1/GPIO3_A7_d	**M22**	I/O	3.3V	DOWN	RMII1_RXD1	RMII1_RXD1
76	SAI2_SDI_M0/ETH_RMII1_RXD0/GPIO3_A6_d	**L22**	I/O	3.3V	DOWN	RMII1_RXD0	RMII1_RXD0
77	GND		G			GND	GND
78	ETH_RMII0_MDIO/DSM_AUD_LP_M1/SAI3_SDO/GPIO2_B7_d	**G21**	I/O	3.3V	DOWN	RMII0_MDIO	RMII0_MDIO
79	ETH_RMII0_MDC/DSM_AUD_LN_M1/SAI3_SDI/GPIO2_B6_d	**F22**	I/O	3.3V	DOWN	RMII0_MDC	RMII0_MDC
80	ETH_RMII0_TXEN/DSM_AUD_RP_M1/SAI3_LRCK/GPIO2_B5_d	**F23**	I/O	3.3V	DOWN	RMII0_TXEN	RMII0_TXEN
81	ETH_RMII0_TXD1/DSM_AUD_RN_M1/SAI3_SCLK/GPIO2_B4_d	**F21**	I/O	3.3V	DOWN	RMII0_TXD1	RMII0_TXD1 (core board series Resistor 22R)
82	ETH_RMII0_TXD0/SPI2_MISO/GPIO2_B3_d	**E22**	I/O	3.3V	DOWN	RMII0_TXD0	RMII0_TXD0 (core board series Resistor 22R)
83	GND		G			GND	GND
84	ETH_RMII0_CLK/SPI2_MOSI/GPIO2_B2_d	**E21**	I/O	3.3V	DOWN	RMII0_CLK	RMII0_CLK (core board series Resistor 22R)
85	ETH_RMII0_RXDVCRS/SAI3_MCLK/GPIO2_C0_d	**G22**	I/O	3.3V	DOWN	RMII0_RXDV_CRS	RMII0_RXDV_CRS
86	ETH_RMII0_RXD1/SPI2_CSN/GPIO2_B1_d	**D23**	I/O	3.3V	DOWN	RMII0_RXD1	RMII0_RXD1

Interface definition

87	ETH_RMII0_RXD0/SPI2_CLK/GPIO2_B0_d	**D21**	I/O	3.3V	DOWN	RMII0_RXD0	RMII0_RXD0
88	GND		G			GND	GND
89	MIPI_DPHY_DSI_TX_CLKN/GPO4_A4_z	**B14**	I/O	-/1.8V	z	MIPI_DPHY_DSI_TX_CLKN	MIPI_DPHY_DSI_TX_CLKN
90	MIPI_DPHY_DSI_TX_CLKP/GPO4_A5_z	**B13**	I/O	-/1.8V	z	MIPI_DPHY_DSI_TX_CLKP	MIPI_DPHY_DSI_TX_CLKP
91	GND		G			GND	GND
92	MIPI_DPHY_DSI_TX_D1N/GPO4_A2_z	**B12**	I/O	-/1.8V	z	MIPI_DPHY_DSI_TX_D1N	MIPI_DPHY_DSI_TX_D1N
93	MIPI_DPHY_DSI_TX_D1P/GPO4_A3_z	**A12**	I/O	-/1.8V	z	MIPI_DPHY_DSI_TX_D1P	MIPI_DPHY_DSI_TX_D1P
94	GND		G			GND	GND
95	MIPI_DPHY_DSI_TX_D0N/GPO4_A0_z	**A11**	I/O	-/1.8V	z	MIPI_DPHY_DSI_TX_D0N	MIPI_DPHY_DSI_TX_D0N
96	MIPI_DPHY_DSI_TX_D0P/GPO4_A1_z	**B11**	I/O	-/1.8V	z	MIPI_DPHY_DSI_TX_D0P	MIPI_DPHY_DSI_TX_D0P
97	GND		G			GND	GND
98	SARADC_IN3/GPIO4_B3_z (OTP)	**B21**	I/O	1.8V	z	SARADC_IN3	ADC3 input
99	SARADC_IN2/GPIO4_B2_z (OTP)	**A21**	I/O	1.8V	z	SARADC_IN2	ADC2 input
100	SARADC_IN1/GPIO4_B1_z (RECOVER) (OTP)	**B20**	I/O	1.8V	z	SARADC_IN1_RECOVER/KEY	ADC1 input (RECOVERY_Key) , Core board pull up Resistor 10K
101	SARADC_IN0/GPIO4_B0_z (BOOT) (OTP)	**A20**	I/O	1.8V	z	SARADC_IN0_BOOT	ADC0 input (BOOT_Key) , Core board pull up Resistor 10K
102	GND		G			GND	GND
103	ACODEC_ADC_INP			1.8V		ACODEC_ADC_INP	ACODEC_IN+ input , Core board series capacitor 1uF
104	ACODEC_ADC_INN			1.8V		ACODEC_ADC_INN	ACODEC_IN- input, Core board series capacitor 1uF

Interface definition

105	SDMMC_D1/TEST_CLK_OUT/GPIO3_A3_d（mount EMMC,this pin NC）	**K22**	I/O	3.3V	DOWN	NC	NC
106	SDMMC_D0/GPIO3_A2_d（mount EMMC,this pin NC）	**K23**	I/O	3.3V	DOWN	NC	NC
107	GND		G			GND	GND
108	SDMMC_CLK/GPIO3_A0_d（mount EMMC,this pin NC）	**K21**	I/O	3.3V	DOWN	NC	NC
109	GND		G			GND	GND
110	SDMMC_CMD/GPIO3_A1_d（mount EMMC,this pin NC）	**J21**	I/O	3.3V	DOWN	NC	NC
111	SDMMC_D3/JTAG_TMS_M0/GPIO3_A5_d（mount EMMC,this pin NC）	**H22**	O	3.3V	DOWN	NC	NC
112	SDMMC_D2/JTAG_TCK_M0/GPIO3_A4_d（mount EMMC,this pin NC）	**H23**	I/O	3.3V	DOWN	NC	NC
113	SAI0_LRCK/RM_IO0/GPIO0_A0_u	**V3**	I/O	3.3V	UP	SDMMC_PWREN	SDMMC_POWR_EN Output, Active H
114	SAI0_MCLK/RM_IO2/GPIO0_A2_u	**W2**	I/O	3.3V	UP	SDMMC_DET	SDMMC_DET Input, Active L
115	USB20_OTG0_VBUSDET (For USB update)	**B18**	I	3.3V		USB20_OTG0_VBUSDET Input	Active H
116	USB20_OTG0_ID	**B17**	I	3.3V		USB20_OTG0_ID Input	USB_OTG_ID,Active L
117	GND		G			GND	GND
118	USB20_OTG0_DM (For USB update)	**B16**	I/O	-		USB20_OTG0_DM	USB20_OTG0_DM
119	USB20_OTG0_DP (For USB update)	**A16**	I/O	-		USB20_OTG0_DP	USB20_OTG0_DP
120	GND		G			GND	GND
121	USB20_OTG1_DM	**B15**	I/O	-		USB20_OTG1_DM	USB20_OTG1_DM
122	USB20_OTG1_DP	**A15**	I/O	-		USB20_OTG1_DP	USB20_OTG1_DP

Interface definition

123	GND		G			GND	GND
124	VO_LCDC_DEN/DSMC_CLKP/FLEXBUS1_D0/GPIO1_A0_d	**B10**	I/O	3.3V	DOWN	LCDC_DEN	LCDC_DEN
125	VO_LCDC_VSYNC/DSMC_CLKN/FLEXBUS1_D1/DSMC_INT0/DSMC_SLV_INT/GPIO1_A1_d	**1A5**	G	3.3V	DOWN	LCDC_VSYNC	LCDC_VSYNC (core board series Resistor 33R)
126	VO_LCDC_HSYNC/DSMC_DQS0/FLEXBUS1_D2/GPIO1_A2_d	**A9**	I/O	3.3V	DOWN	LCDC_HSYNC	LCDC_HSYNC (core board series Resistor 33R)
127	GND		G			GND	GND
128	VO_LCDC_CLK/DSMC_D0/FLEXBUS1_D3/GPIO1_A3_d	**B9**	I/O	3.3V	DOWN	LCDC_CLK	LCDC_CLK (core board series Resistor 22R)
129	GND		G			GND	GND
130	VO_LCDC_D23/DSMC_D1/FLEXBUS1_D4/GPIO1_A4_d	**B8**	I/O	3.3V	DOWN	LCD_D23	LCD_D23
131	VO_LCDC_D22/DSMC_D2/FLEXBUS1_D5/GPIO1_A5_d	**1A4**	I/O	3.3V	DOWN	LCD_D22	LCD_D22
132	VO_LCDC_D21/DSMC_D3/FLEXBUS1_D6/GPIO1_A6_d	**A7**	I/O	3.3V	DOWN	LCD_D21	LCD_D21
133	VO_LCDC_D20/DSMC_D4/FLEXBUS1_D7/GPIO1_A7_d	**B7**	I/O	3.3V	DOWN	LCD_D20	LCD_D20
134	VO_LCDC_D19/DSMC_D5/FLEXBUS1_D8/FLEXBUS0_CSN_M0/GPIO1_B0_d	**1A3**	I/O	3.3V	DOWN	LCD_D19	LCD_D19
135	VO_LCDC_D18/DSMC_CSN1/FLEXBUS1_D9/FLEXBUS1_CSN_M0/UART5_CTSN_M1/RM_IO24/GPIO1_B1_d	**1A2**	I/O	3.3V	DOWN	LCD_D18	LCD_D18
136	VO_LCDC_D17/DSMC_INT2/FLEXBUS1_D10/FLEXBUS0_D15/FLEXBUS0_CSN_M1/SAI2_SCLK_M1/RM_IO25/GPIO1_B2_d	**A5**	I/O	3.3V	DOWN	LCD_D17	LCD_D17

T-CHIP INTELLIGENCE TECHNOLOGY

Contact Us
(+86)18688117175

E-mail
global@t-firefly.com

Website
www.t-firefly.com

Address
Room 2101, Hongyu Building, #57 Zhongshan 4Rd, East District, Zhongshan, Guangdong, China.