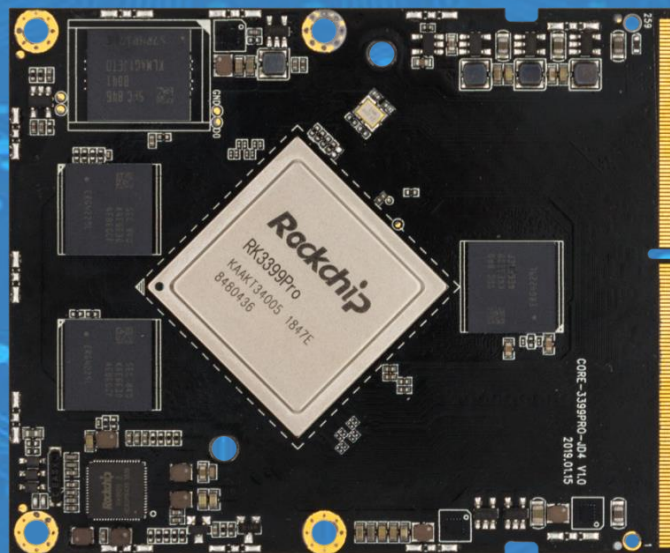


# Core-3399Pro-JD4

六核高性能AI核心板

V1.2



天启智能科技有限公司  
[www.t-firefly.com](http://www.t-firefly.com)

## 更新记录

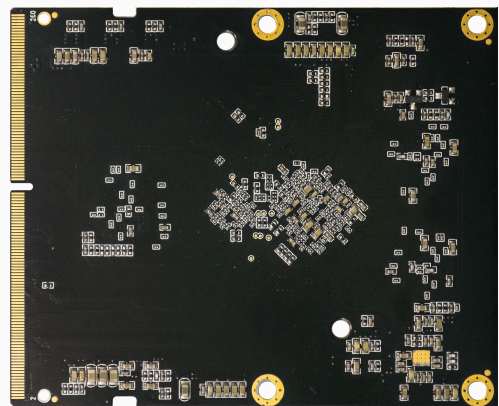
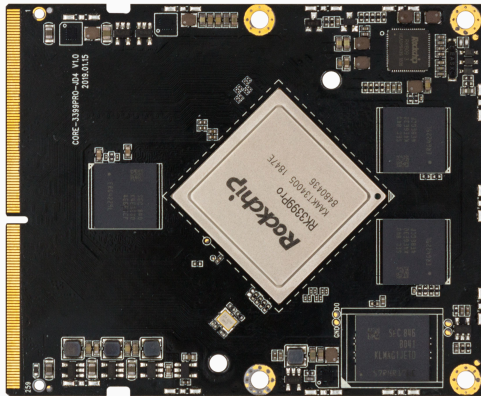
版本	更新日期	更新内容
V1.0	2019-04-26	原始版本
V1.1	2020-09-17	更新接口定义
V1.2	2021-04-25	更新接口定义

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### 一、产品简介

采用高性能 AI 处理芯片 RK3399Pro，集成神经网络处理器 NPU，算力高达 3.0Tops，兼容多种 AI 框架，可与底板组合，构成一块完整的行业应用主板，灵活应用于各种智能产品。



#### 高性能 AI 处理器 RK3399Pro

采用了 ARM 双核 Cortex-A72 + 四核 Cortex-A53 的大小核处理器架构，主频高达 1.8GHz，集成 Mali-T860 MP4 四核图形处理器，通用运算性能强悍。

#### 强大的硬件解码能力

支持 DP1.2、HDMI 2.0、MIPI-DSI、eDP 多种显示输出接口，支持双屏同显/双屏异显，支持 4K@60fps VP9/H.265、4K@30fps H.264 和 1080P@30fps多格式 (VC-1, MPEG-1/2/4)视频解码、1080P@30fps H.264/AVC/VP8视频编码

#### 支持多个操作系统

支持 Android、Linux+QT、Ubuntu 多个操作系统，性能稳定可靠。

#### 组成行业应用主板

Core-3399Pro-JD4 核心板与底板组合，构成完整的高性能行业应用主板，扩展接口更丰富，性能更强大，可直接应用到各种智能产品中，加速产品落地。

#### 超强 AI 运算性能 NPU

集成 AI 神经网络处理器 NPU，支持 8Bit/16Bit 运算，算力高达 3.0Tops，满足视觉、音频等各类 AI 应用。

#### 多种 AI 框架支持

兼容多种 AI 框架，支持 TensorFlow Lite/Android NN API，AI 软件工具支持对 Caffe / TensorFlow 模型的导入及映射、优化，让开发者便捷地运用 AI 技术。

#### 丰富的扩展接口

拥有 I2C、SPI、UART、ADC、PWM、GPIO、PCIe、USB3.0、I2S 等丰富接口。

#### 应用广泛

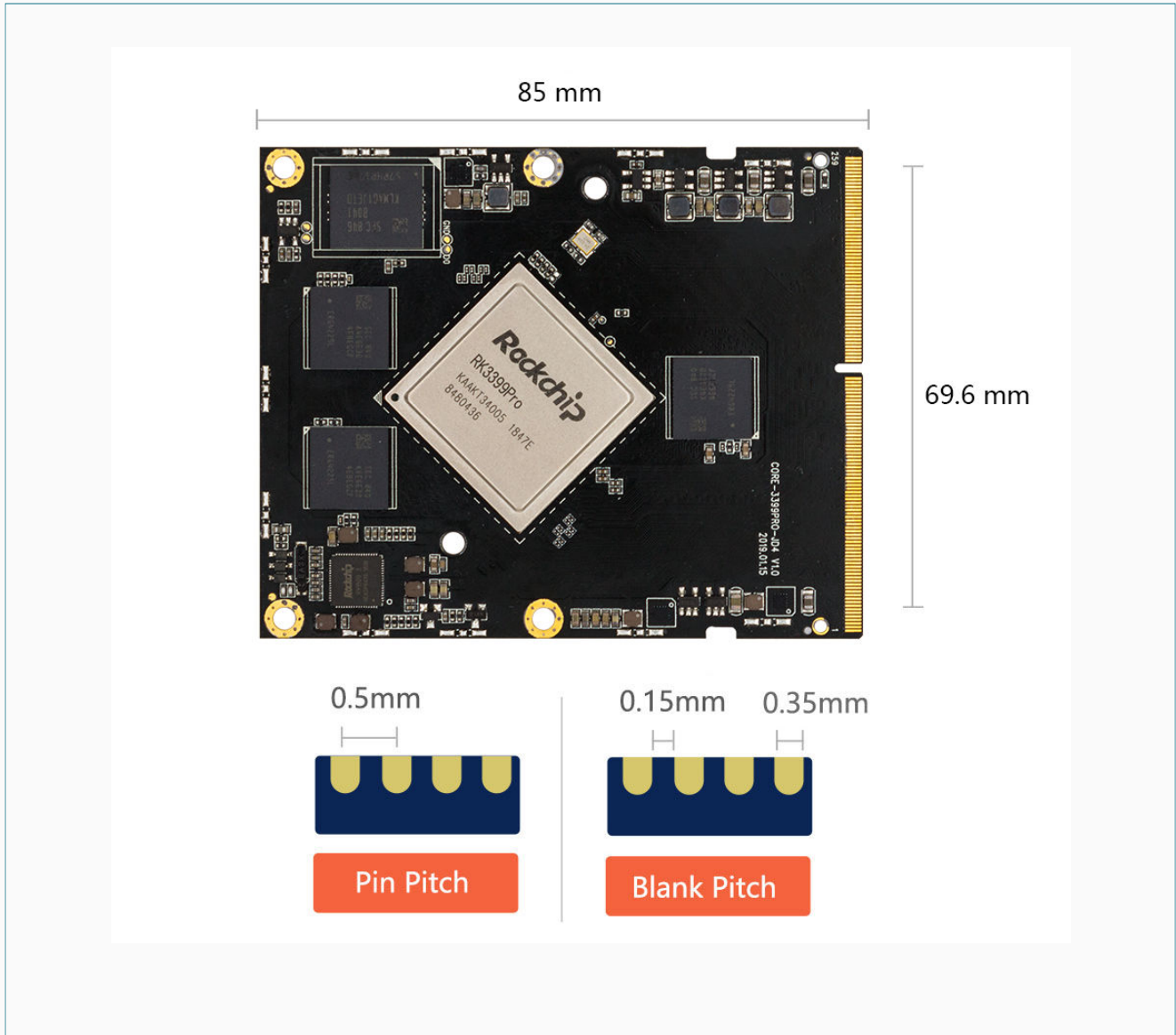
广泛适用于集群服务器、高性能计算/存储、计算机视觉、边缘计算、商显一体设备、医疗健康设备、自动售货机、工业电脑等各 AI 应用领域



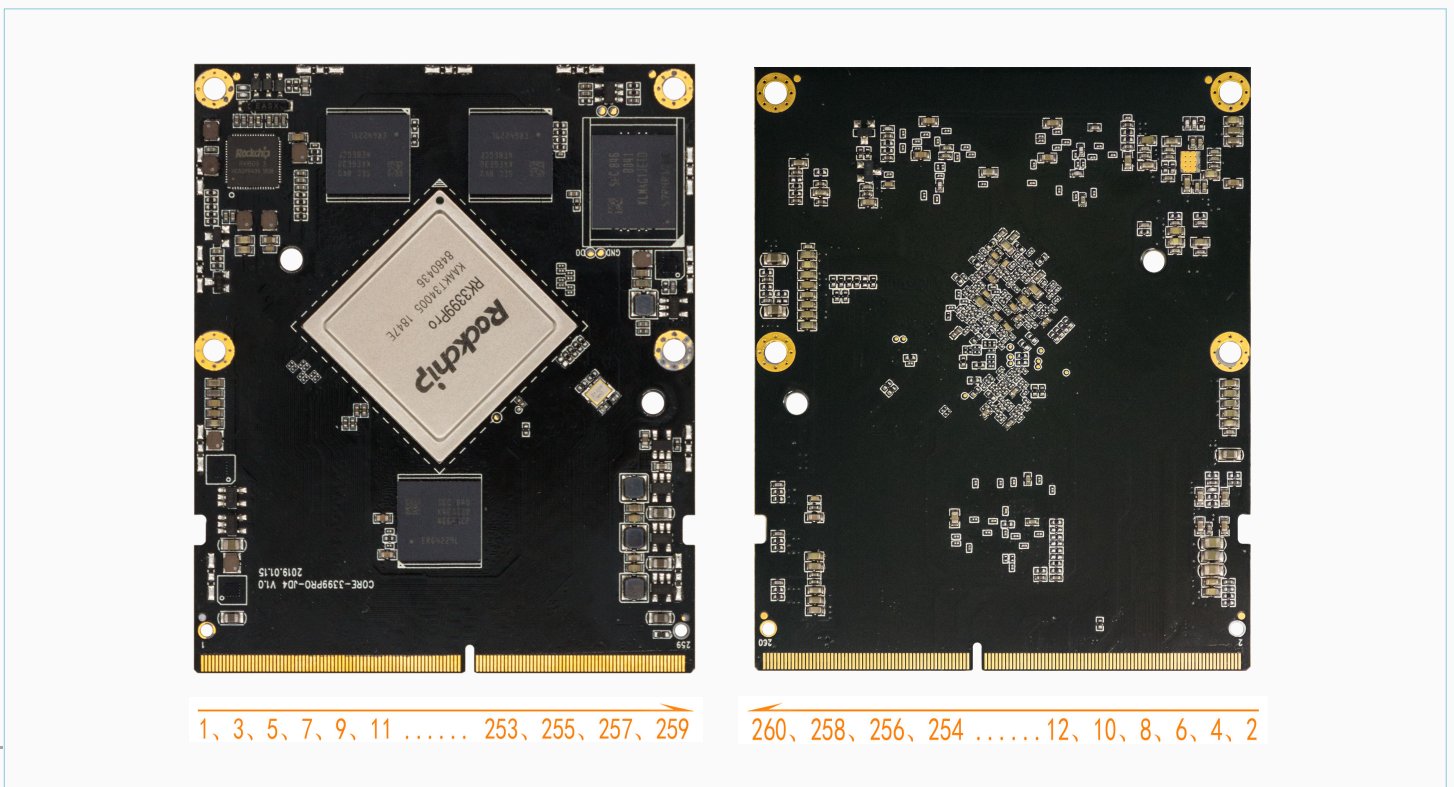
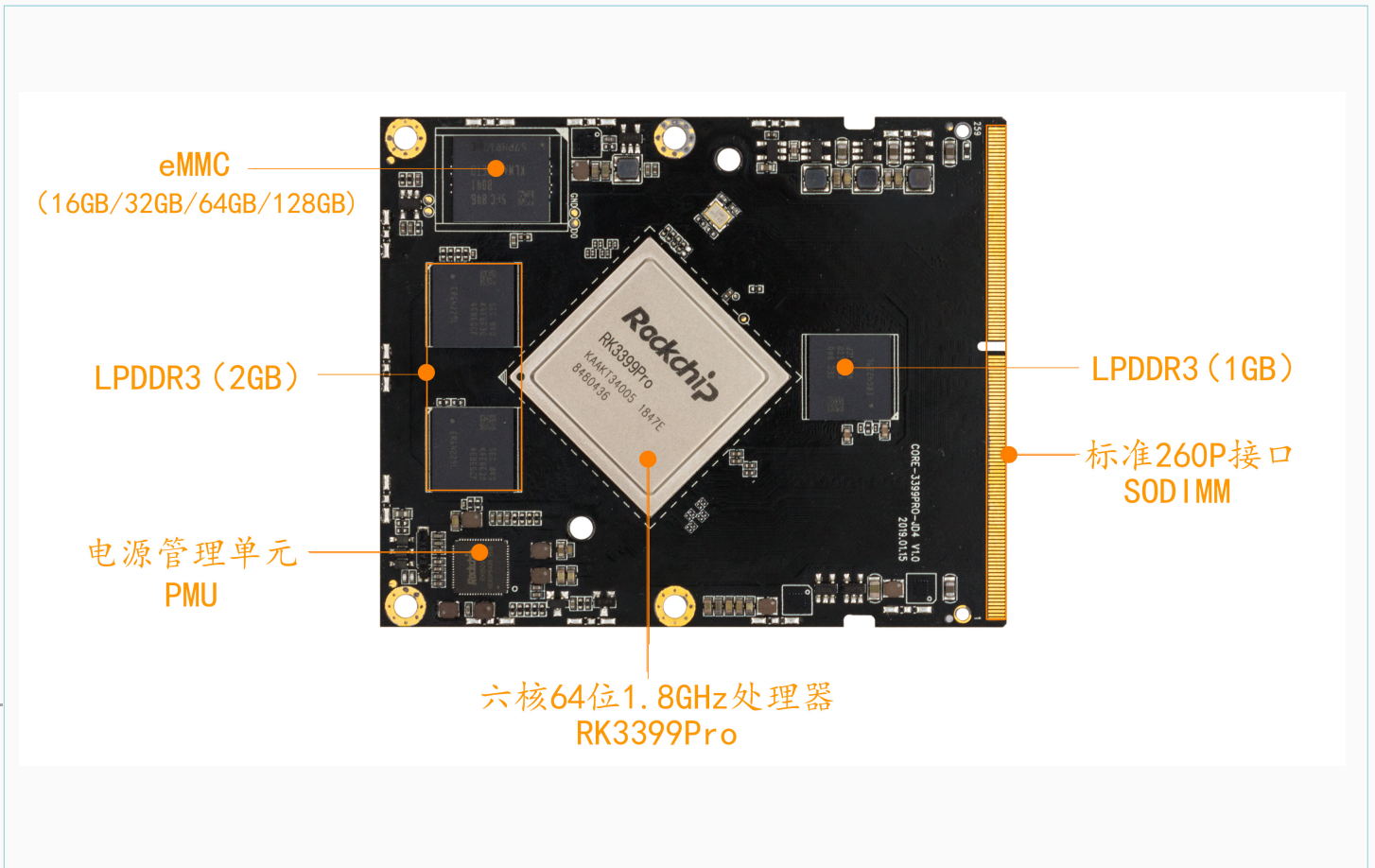
## 二、规格参数

基本参数	
主控芯片	Rockchip RK3399Pro
处理器	双 Cortex-A72+四 Cortex-A53 大小核 CPU 结构, 频率最高 1.8GHz
图形处理器	ARM® Mali-T860 MP4 四核 GPU 支持 OpenGL ES1.1/2.0/3.0/3.1, OpenVG1.1, OpenCL, DX11 支持 AFBC (帧缓冲压缩)
NPU	内置运算性能强悍的神经网络处理器 NPU: - 支持 8bit/16bit 运算, 运算性能高达 3.0TOPS - 相较于 GPU 作为 AI 运算单元的大型芯片方案, 功耗不到 GPU 所需要的 1% - 可直接加载 Caffe / Mxnet / TensorFlow 模型 - 提供 AI 开发工具: 支持模型快速转换、支持开发板端侧转换 API、支持 TensorFlow / TF Lite / Caffe / ONNX / Darknet 等模型 - 提供 AI 应用开发接口: 支持 Android NN API、提供 RKNN 跨平台 API、Linux 支持 TensorFlow 开发
视频处理器	硬解码: 4K@60fps H.265/VP9、4K@30fps H.264 视频解码、 1080P@60fps(VC-1, MPEG-1/2/4) 多格式视频解码 硬编码: 1080P@30fps H.264/AVC/VP8 视频编码 视频后期处理器: 反交错、去噪、边缘/细节/色彩优化
内存	LPDDR3 3GB (NPU 1GB + CPU 2GB)、LPDDR3 6GB (NPU 2GB + CPU 4GB)
存储器	高速 eMMC 5.1 (16GB/32GB/64GB/128GB 可选) 支持 TF 卡扩展
硬件特性	
以太网	1 × GMAC, 提供 RGMII/RMII 接口, 支持 10/100/1000Mbps 数据传输速率
显示	1 × HDMI2.0 (支持 4K@60Hz 输出 和 HDCP 1.4/2.2) 2 × MIPI-DSI (支持单通道 2560×1600@60fps 输出) 1 × eDP 1.2 (4 lanes with 10.8Gbps) 支持双屏同显、双屏异显
音频	1 × HDMI2.0 音频输出 1 × I2S 用于音频输入输出 (支持 8 路数字麦克风阵列输入) 1 × Speaker 喇叭 (8Ω, 1.3W, 单声道) 1 × 耳机输出 1 × Mic 音频输入
摄像头	2 × MIPI-CSI 摄像头接口 (内置双硬件 ISP, 最高支持单 13Mpixel 或 双 8Mpixel)
USB	2 × USB2.0 HOST、1 × USB3.0 OTG
PCIe	1 × PCIe2.1
扩展接口	UART×5、ADC×4、I2C×9、PWM×3、GPIOs、SPI×5
电源	DC 输入电压 5V
功耗	休眠功耗: 2.6W(5V/520mA), 典型功耗: 3.75W(5V/750mA), 最大功耗: 6W(5V/1200mA)
系统软件	
系统支持	Android、Linux+QT、Ubuntu
软件支持	提供 AI 开发工具: 支持模型快速转换、支持开发板端侧转换 API、支持 TensorFlow / TF Lite / Caffe / ONNX / Darknet 等模型 提供 AI 应用开发接口: 支持 Android NN API、提供 RKNN 跨平台 API、Linux 支持 TensorFlow 开发
外观规格	
核心板尺寸	69.6mm × 85.0mm
接口类型	金手指 (SODIMM 260P 标准接口, 0.5mm 间距)
PCB 规格	10 层板设计

### 三、核心板尺寸

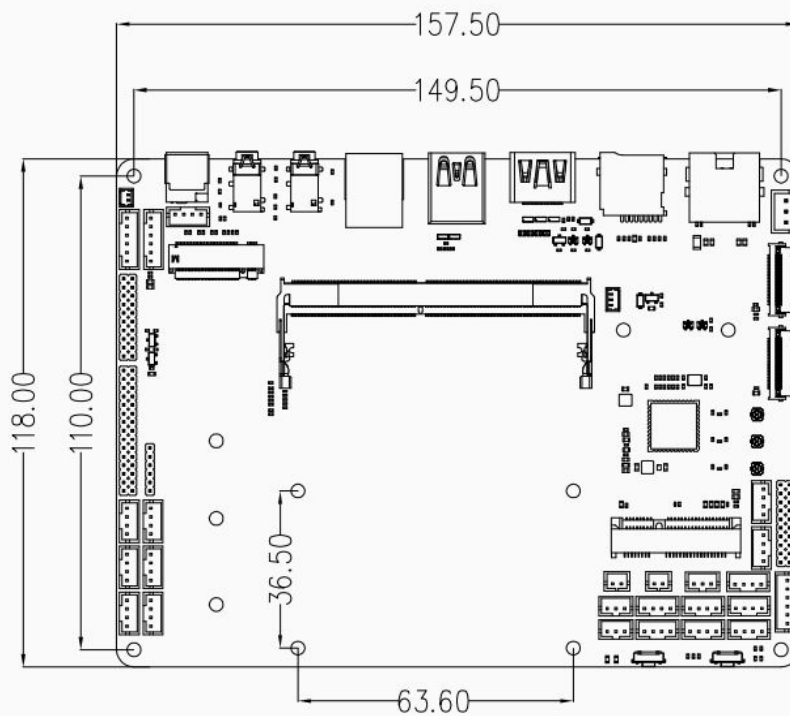
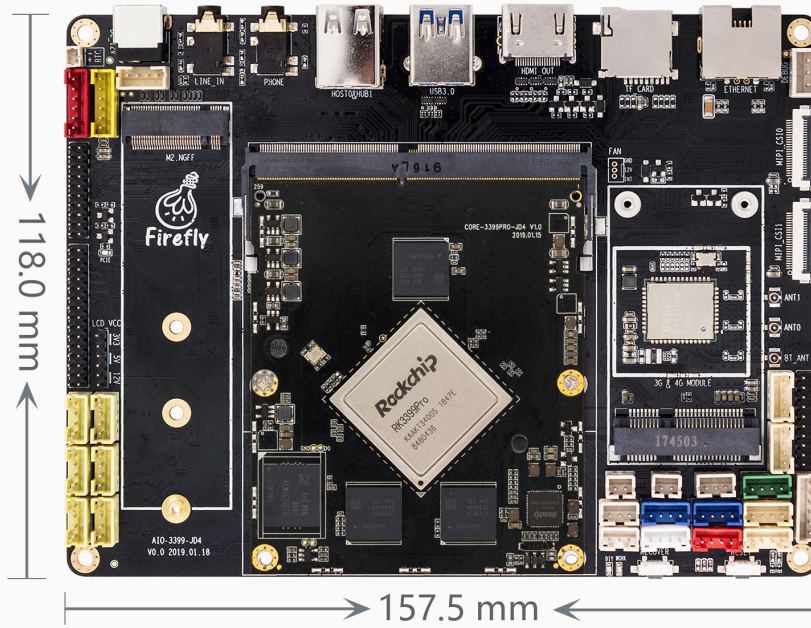


### 四、核心板接口描述

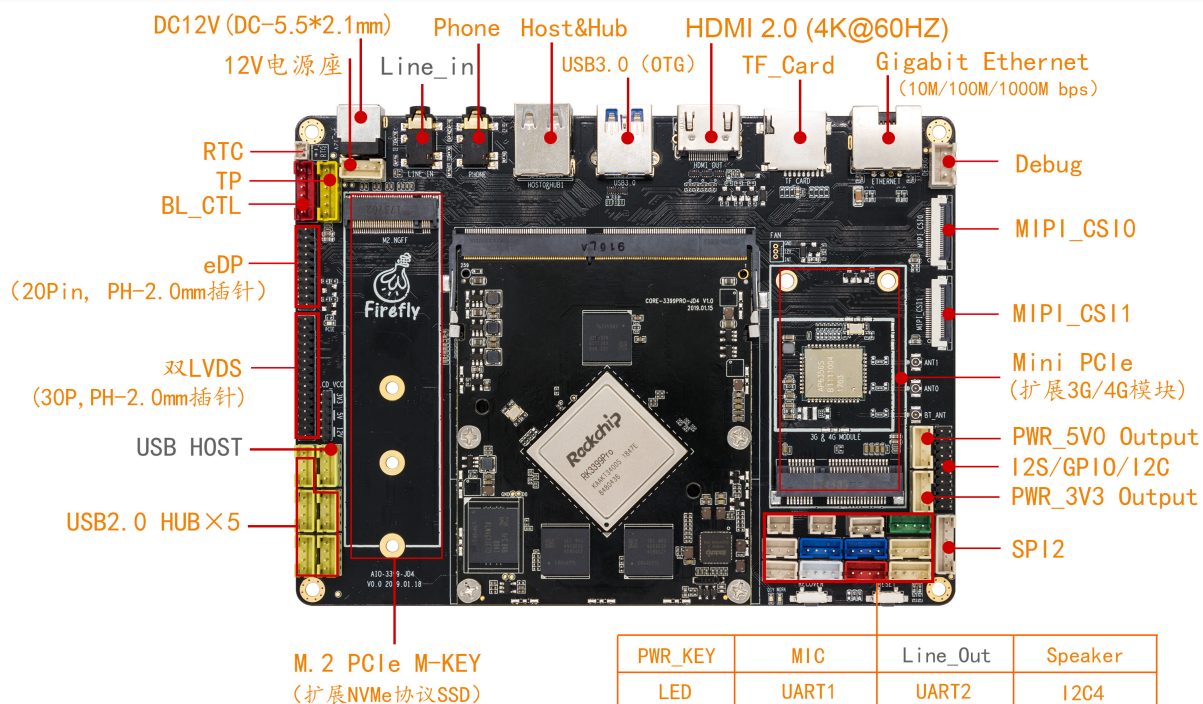




### 五、主板尺寸



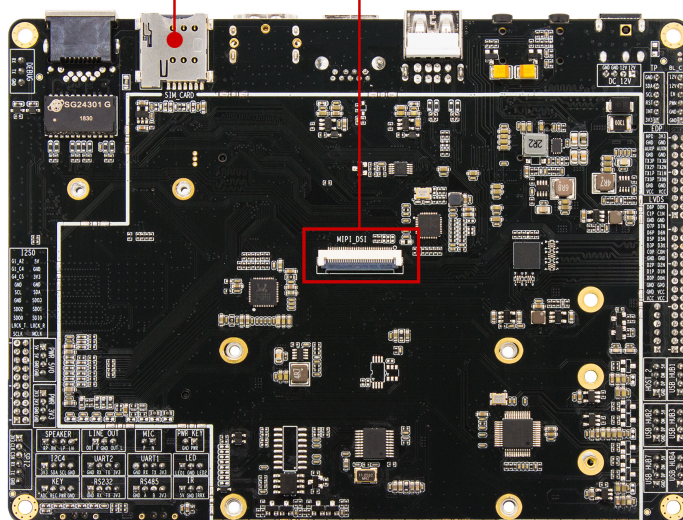
## 六、主板接口描述



备注：此底板兼容Core-3399ProJD4 和 Core-3399JD4

当核心板为Core-3399ProJD4（即本产品）时，不支持灰色标注的 USB Host、Line\_in、Line\_Out功能

SIM卡 (MicroSIM标准) MIPI-DSI



## 七、接口定义

Notes1:

①: Pad types: I = input, O = output, I/O = input/output (bidirectional), G = Ground,  
P = power supply, DOWN = Internal pull down, UP = Internal pull up  
0 = Low level 1 = High level

Part A	PIN	Core board pin definition	Pad type	IO Pull	Function for Floor(MB-3399PRO-JD4)	Default function description	IO Power domain	RK3399Pro Pin Number	RK3399Pro Pin Name
	1	GND_1	G		GND	GND			
	3	GPIO0_A1/DDR10_PWR0FF/TCPD_CCDB_EN_u.1.8V	I/O	UP	WORK_LED	System LED control H:Enable, L:Disable	1.8V	L34	GPIO0_A1/DDR10_PWR0FF/TCPD_CCDB_EN
	5	GPIO1_B5_d.1.8V	I/O	DOWN	DIY_LED	Diy led control H:Enable, L:Disable	1.8V	D38	GPIO1_B5
	7	GPIO4_D2_d.3.0V	I/O	DOWN	VCC5V0_HOST_EN	Host usb 5v power enable H:Enable, L:Disable	3.0V	AG4	GPIO4_D2
	9	GPIO4_C5/SPDIF_TX_d.3.0V	I/O	DOWN	VCC5V0_TYPEC0_EN	OTG 5v power enable H:Enable, L:Disable	3.0V	AM1	GPIO4_C5/SPDIF_TX
	11	GPIO4_D1/DP_HOTPLUG_d.3.0V	I/O	DOWN	LVDS_RESX	LVDS Reset	3.0V	AK4	GPIO4_D1/DP_HOTPLUG
	13	GPIO1_B4/I2C4_SCL_u.3.0V	I/O	UP	I2C4_SCL	I2C4 clock, Core board internal pull up Resistor 4.7K	3.0V	G35	GPIO1_B4/I2C4_SCL
	15	GPIO1_B3/I2C4_SDA_u.3.0V	I/O	UP	I2C4_SDA	I2C4 data, Core board internal pull up Resistor 4.7K	3.0V	F36	GPIO1_B3/I2C4_SDA
	17	GPIO4_D6_d.3.0V	I/O	DOWN	LCD_EN	Lcd enable	3.0V	AF4	GPIO4_D6
	19	GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOUR_CE3_d.1.8V	I/O	DOWN	CAM_PWR	Camera power enable	1.8V	L35	GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOUR_CE3
	21	GPIO1_A2/ISPO_FLASHTRIGIN/ISP1_FLASHTRIGIN/TCPD_CC1_VCONN_EN_d.1.8V	I/O	DOWN	MIPI_PWR_EN	MIPI power enable	1.8V	D40	GPIO1_A2/ISPO_FLASHTRIGIN/ISP1_FLASHTRIGIN/TCPD_CC1_VCONN_EN
	23	NC_1							
	25	GPIO1_C4/I2C8_SDA_u.1.8V	I/O	UP	MIPI_RST	Mipi reset	1.8V	J33	GPIO1_C4/I2C8_SDA
	27	GPIO1_C5/I2C8_SCL_u.1.8V	I/O	UP	LCD_BL_EN	LCD back-light enable	1.8V	H32	GPIO1_C5/I2C8_SCL
	29	GPIO1_B2/SPI1_CSNO/PMCU_JTAG_TMS_u.1.8V	I/O	UP	GPIO1_B2/SPI1_CSNO	GPIO/SPI bus port 1	1.8V	H35	GPIO1_B2/SPI1_CSNO/PMCU_JTAG_TMS
	31	GPIO1_B0/SPI1_TXD/UART4_TX_u.1.8V	I/O	UP	GPIO1_B0/SPI1_TXD/UART4_TX	GPIO/SPI bus port 1,UART4 serial port	1.8V	B39	GPIO1_B0/SPI1_TXD/UART4_TX
	33	GPIO1_A7/SPI1_RXD/UART4_RX_u.1.8V	I/O	UP	GPIO1_A7/SPI1_RXD/UART4_RX	GPIO/SPI bus port 1,UART4 serial port	1.8V	F37	GPIO1_A7/SPI1_RXD/UART4_RX
	35	GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK_u.1.8V	I/O	UP	GPIO1_B1/SPI1_CLK	GPIO/SPI bus port 1	1.8V	G36	GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK
	37	GPIO4_D4_d.3.0V	I/O	DOWN	TP_RST	external TP reset output	3.0V	AM5	GPIO4_D4
	39	NC_2							
	41	GPIO0_B1/PMU02_VOLSEL_d.1.8V	I/O	DOWN	SPK_CTL_H	Amplifier enable	1.8V	L36	GPIO0_B1/PMU02_VOLSEL
	43	GND_2	G		GND	GND			
	45	MIPI_TX1/RX1_D0P	I/O		MIPI_TX1/RX1_D0P	MIPI-DSI1/CSI1 differential lane 0 positive		AN2	MIPI_TX1/RX1_D0P
	47	MIPI_TX1/RX1_D0N	I/O		MIPI_TX1/RX1_D0N	MIPI-DSI1/CSI1 differential lane 0 negative		AN1	MIPI_TX1/RX1_D0N
	49	MIPI_TX1/RX1_D1P	I/O		MIPI_TX1/RX1_D1P	MIPI-DSI1/CSI1 differential lane 1 positive		AP2	MIPI_TX1/RX1_D1P
	51	MIPI_TX1/RX1_D1N	I/O		MIPI_TX1/RX1_D1N	MIPI-DSI1/CSI1 differential lane 1 negative		AP1	MIPI_TX1/RX1_D1N
	53	MIPI_TX1/RX1_CLKP	I/O		MIPI_TX1/RX1_CLKP	MIPI-DSI1/CSI1 differential clock lane positive		AR2	MIPI_TX1/RX1_CLKP
	55	MIPI_TX1/RX1_CLKN	I/O		MIPI_TX1/RX1_CLKN	MIPI-DSI1/CSI1 differential clock lane negative		AR1	MIPI_TX1/RX1_CLKN
	57	MIPI_TX1/RX1_D2P	I/O		MIPI_TX1/RX1_D2P	MIPI-DSI1/CSI1 differential lane 2 positive		AT2	MIPI_TX1/RX1_D2P
	59	MIPI_TX1/RX1_D2N	I/O		MIPI_TX1/RX1_D2N	MIPI-DSI1/CSI1 differential lane 2 negative		AT1	MIPI_TX1/RX1_D2N
	61	MIPI_TX1/RX1_D3P	I/O		MIPI_TX1/RX1_D3P	MIPI-DSI1/CSI1 differential lane 3 positive		AU2	MIPI_TX1/RX1_D3P
	63	MIPI_TX1/RX1_D3N	I/O		MIPI_TX1/RX1_D3N	MIPI-DSI1/CSI1 differential lane 3 negative		AU1	MIPI_TX1/RX1_D3N
	65	GND_3	G		GND	GND			
	67	MIPI_RX0_D3P	I		MIPI_RX0_D3P	MIPI-CSIO differential lane 3 positive		AV2	MIPI_RX0_D3P
	69	MIPI_RX0_D3N	I		MIPI_RX0_D3N	MIPI-CSIO differential lane 3 negative		AV1	MIPI_RX0_D3N
	71	MIPI_RX0_D2P	I		MIPI_RX0_D2P	MIPI-CSIO differential lane 2 positive		AW2	MIPI_RX0_D2P
	73	MIPI_RX0_D2N	I		MIPI_RX0_D2N	MIPI-CSIO differential lane 2 negative		AW1	MIPI_RX0_D2N
	75	MIPI_RX0_CLKP	I		MIPI_RX0_CLKP	MIPI-CSIO differential clock lane positive		AW3	MIPI_RX0_CLKP
	77	MIPI_RX0_CLKN	I		MIPI_RX0_CLKN	MIPI-CSIO differential clock lane negative		AY3	MIPI_RX0_CLKN
	79	MIPI_RX0_D1P	I		MIPI_RX0_D1P	MIPI-CSIO differential lane 1 positive		AW4	MIPI_RX0_D1P
	81	MIPI_RX0_D1N	I		MIPI_RX0_D1N	MIPI-CSIO differential lane 1 negative		AY4	MIPI_RX0_D1N
	83	MIPI_RX0_D0P	I		MIPI_RX0_D0P	MIPI-CSIO differential lane 0 positive		AW5	MIPI_RX0_D0P
	85	MIPI_RX0_D0N	I		MIPI_RX0_D0N	MIPI-CSIO differential lane 0 negative		AY5	MIPI_RX0_D0N
	87	GND_4	G		GND	GND			
	89	HDMI_PORT_HPD	I		HDMI_HPD	HDMI Hot Plug Detection interrupt with 5V tolerance, Core board internal series resistance 1K		AE15	HDMI_HPD
	91	GPIO4_C0/I2C3_SDA/UART2B_RX_u.3.0V	I/O	UP	I2C3_SDA_HDMI	I2C serial port 3,for HDMI, need external pull-up	3.0V	AP6	GPIO4_C0/I2C3_SDA/UART2B_RX
	93	GPIO4_C1/I2C3_SCL/UART2B_TX_u.3.0V	I/O	UP	I2C3_SCL_HDMI	I2C serial port 3,for HDMI, need external pull-up	3.0V	AK2	GPIO4_C1/I2C3_SCL/UART2B_TX
	95	GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG_u.3.0V	I/O	UP	HDMI_CEC	HDMI CEC communication	3.0V	AD7	GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG
	97	GND_5	G		GND	GND			
	99	HDMI_TXCN	O		HDMI_TXCN	HDMI differential pixel clock negative, Core board internal series resistance 2.2R		AY6	HDMI_TXCN
	101	HDMI_TXCP	O		HDMI_TXCP	HDMI differential pixel clock positive, Core board internal series resistance 2.2R		AW6	HDMI_TXCP
	103	HDMI_TXON	O		HDMI_TXON	HDMI channel 0 differential serial data negative, Core board internal series resistance 2.2R		AY7	HDMI_TXON
	105	HDMI_TXOP	O		HDMI_TXOP	HDMI channel 0 differential serial data positive, Core board internal series resistance 2.2R		AW7	HDMI_TXOP
	107	HDMI_TX1N	O		HDMI_TX1N	HDMI channel 1 differential serial data negative, Core board internal series resistance 2.2R		AY8	HDMI_TX1N
	109	HDMI_TX1P	O		HDMI_TX1P	HDMI channel 1 differential serial data positive, Core board internal series resistance 2.2R		AW8	HDMI_TX1P
	111	HDMI_TX2N	O		HDMI_TX2N	HDMI channel 2 differential serial data negative, Core board internal series resistance 2.2R		AY9	HDMI_TX2N



113	HDMI_TX2P	0		HDMI_TX2P	HDMI channel 2 differential serial data positive . Core board internal series resistance 2.2R		AW9	HDMI_TX2P
115	GND_6	G		GND	GND			
117	TYPECO_AUXP_PD_PU			TYPECO_AUXP_PD_PU	TYPECO AUX pull-up/pull-down polarityreversal pins. (not connect)		AH17	TYPECO_AUXP_PD_PU
119	TYPECO_AUXM_PU_PD			TYPECO_AUXM_PU_PD	TYPECO AUX pull-up/pull-down polarityreversal pins.(not connect)		AG17	TYPECO_AUXM_PU_PD
121	TYPECO_AUXM	I/O		TYPECO_AUXM	TYPECO AUX differential TX/RX serial data(not connect)		AU11	TYPECO_AUXM
123	TYPECO_AUXP	I/O		TYPECO_AUXP	TYPECO AUX differential TX/RX serial data(not connect)		AT11	TYPECO_AUXP
125	TYPECO_RX1M	I		USB3_SSRXN	TYPECO negative half of first Super Speed RX differential pair		AY11	TYPECO_RX1M
127	TYPECO_RX1P	I		USB3_SSRXP	TYPECO positive half of first Super Speed RX differential pair		AW11	TYPECO_RX1P
129	TYPECO_TX1P	0		USB3_SSTXP	TYPECO positive half of first Super Speed TX differential pair.		AY12	TYPECO_TX1P
131	TYPECO_TX1M	0		USB3_SSTXN	TYPECO negative half of first Super Speed TX differential pair		AW12	TYPECO_TX1M
133	TYPECO_DP			TYPECO_DP	TYPECO Data Plus port(USB_DP for system update)		AT12	TYPECO_DP
135	TYPECO_DM			TYPECO_DM	TYPECO Data Minus port(USB_DM for system update)		AU12	TYPECO_DM
137	TYPECO_RX2M	I		TYPECO_RX2M	TYPECO negative half of second SuperSpeedRX differential pair.(not connect)		AV13	TYPECO_RX2M
139	TYPECO_RX2P	I		TYPECO_RX2P	TYPECO positive half of second SuperSpeedRX differential pair.(not connect)		AW13	TYPECO_RX2P
141	TYPECO_TX2P	0		TYPECO_TX2P	TYPECO positive half of second SuperSpeedTX differential pair.(not connect)		AV14	TYPECO_TX2P
143	TYPECO_TX2M	0		TYPECO_TX2M	TYPECO negative half of second SuperSpeedTX differential pair.(not connect)		AW14	TYPECO_TX2M
145	TYPECO_U2VBUSDET	I		TYPECO_U2VBUSDET	TYPECO connected/vbus power detect for USB2.0		AR17	TYPECO_U2VBUSDET
147	GND_7	G		GND	GND			
149	PCIE_RX3_P	I		PCIE_RX3_P	PCIE differential lane 3 positive input		V40	PCIE_RX3_P
151	PCIE_RX3_N	I		PCIE_RX3_N	PCIE differential lane 3 negative input		V39	PCIE_RX3_N
153	PCIE_TX3P	0		PCIE_TX3P	PCIE differential lane 3 positive output		U40	PCIE_TX3P
155	PCIE_TX3N	0		PCIE_TX3N	PCIE differential lane 3 negative output		U39	PCIE_TX3N
157	PCIE_RX2_P	I		PCIE_RX2_P	PCIE differential lane 2 positive input		T40	PCIE_RX2_P
159	PCIE_RX2_N	I		PCIE_RX2_N	PCIE differential lane 2 negative input		T39	PCIE_RX2_N
161	PCIE_TX2P	0		PCIE_TX2P	PCIE differential lane 2 positive output		V37	PCIE_TX2P
163	PCIE_TX2N	0		PCIE_TX2N	PCIE differential lane 2 negative output		V36	PCIE_TX2N
165	PCIE_RX1_P	I		PCIE_RX1_P	PCIE differential lane 1 positive input		U37	PCIE_RX1_P
167	PCIE_RX1_N	I		PCIE_RX1_N	PCIE differential lane 1 negative input		U36	PCIE_RX1_N
169	PCIE_TX1P	0		PCIE_TX1P	PCIE differential lane 1 positive output		R40	PCIE_TX1P
171	PCIE_TX1N	0		PCIE_TX1N	PCIE differential lane 1 negative output		R39	PCIE_TX1N
173	PCIE_RX0_P	I		PCIE_RX0_P	PCIE differential lane 0 positive input		P40	PCIE_RX0_P
175	PCIE_RX0_N	I		PCIE_RX0_N	PCIE differential lane 0 negative input		P39	PCIE_RX0_N
177	PCIE_TX0P	0		PCIE_TX0P	PCIE differential lane 0 positive output		R36	PCIE_TX0P
179	PCIE_TX0N	0		PCIE_TX0N	PCIE differential lane 0 negative output		R37	PCIE_TX0N
181	PCIE_RCLK_100M_N	0		PCIE_REF_CLKN	PCIE 100MHz reference clock as input to PLL		P37	PCIE_RCLK_100M_N
183	PCIE_RCLK_100M_P	0		PCIE_REF_CLKP	PCIE 100MHz reference clock as input to PLL		P36	PCIE_RCLK_100M_P
185	GND_8	G		GND	GND			
187	HOSTO_DP			HOSTO_DP	USB HOSTO Data Plus port		M39	USB2O_HOSTO_DP
189	HOSTO_DM			HOSTO_DM	USB HOSTO Data Minus port		M40	USB2O_HOSTO_DN
191	GND_9	G		GND	GND			
193	HOST1_DP			HOST1_DP	USB HOST1 Data Plus port		L39	USB2O_HOST1_DP
195	HOST1_DM			HOST1_DM	USB HOST1 Data Minus port		L40	USB2O_HOST1_DN
197	GND_10	G		GND	GND			
199	EDP_TX3N	0		EDP_TX3N	eDP differential lane 3 negative output		B32	EDP_TX3N
201	EDP_TX3P	0		EDP_TX3P	eDP differential lane 3 positive output		A33	EDP_TX3P
203	EDP_TX2N	0		EDP_TX2N	eDP differential lane 2 negative output		B31	EDP_TX2N
205	EDP_TX2P	0		EDP_TX2P	eDP differential lane 2 positive output		A31	EDP_TX2P
207	EDP_TX1N	0		EDP_TX1N	eDP differential lane 1 negative output		B30	EDP_TX1N
209	EDP_TX1P	0		EDP_TX1P	eDP differential lane 1 positive output		A30	EDP_TX1P
211	EDP_TX0N	0		EDP_TX0N	eDP differential lane 0 negative output		B29	EDP_TX0N
213	EDP_TX0P	0		EDP_TX0P	eDP differential lane 0 positive output		A29	EDP_TX0P
215	EDP_AUXN	I/O		EDP_AUXN	eDP differential AUX channel positive output		B28	EDP_AUXN
217	EDP_AUXP	I/O		EDP_AUXP	eDP differential AUX channel negative output		A28	EDP_AUXP
219	GND_11	G		GND	GND			
221	POWER_ON	I		POWER_ON	Power on Signal Input, External connection Power key , active low			
223	PMIC_VDC	P		VCC_5V_S	PMIC_EN(rising edge triggering start): Input Voltage 3V-5.5V , MAX input current 50mA			
225	VCC_1V8_S3	P		VDD10_WL(LDO)	Output Voltage 1.8V, MAX output current 200mA			
227	VCC10_3V3_S0	P		VCC_LAN(DCDC)	Output Voltage 3.3V, MAX output current 500mA			
229	VCCA1V8_CODEC_1	P		VCCA1V8_CODEC(LDO)	Output Voltage 1.8V, MAX output current 200mA			
231	VCCA3V0_CODEC_1	P		VCCA3V0_CODEC(LDO)	Output Voltage 3.0V, MAX output current 200mA			
233	VCC_5V_S	P		VCC_5V_S	Input Voltage 3.3V-5.5V , MAX input current 50mA			
235	VCC3V3_SYS	P		VCC3V3_SYS(DCDC)	Output Voltage 3.3V, MAX output current 500mA			
237	HP_SNS	G		HP_SNS	Reference ground for the headphone			



239	MIC2_IN	I		MIC2_IN	Negative input of the Microphone				
241	MIC1_IN	I		MIC1_IN	Positive input of the Microphone				
243	GND_12	G		GND	Power ground				
245	GND_13	G		GND					
247	GND_14	G		GND					
249	GND_15	G		GND					
251	VCC_SYS_1	P		VCC5V0_SYS					
253	VCC_SYS_3	P		VCC5V0_SYS	System Power supply Input Voltage : Min 4.8V, Typ 5.0V, Max 5.2V Input current: Typ 1000mA ;Max 2000mA				
255	VCC_SYS_5	P		VCC5V0_SYS					
257	VCC_SYS_7	P		VCC5V0_SYS					
259	VCC_SYS_9	P		VCC5V0_SYS					
Part B	PIN	Core board pin definition	Pad type	IO Pull	Function for Floor(MB-3399PRO-JD4)	Defual function description	IO Power domain	RK3399Pro Pin Number	RK3399Pro Pin Name
	2	GND_16	G		GND	GND			
	4	GPIO3_D0/I2S0_SCLK_d_1.8V	I/O	DOWN	I2S0_SCLK	I2S0 serial clock , for audio codec	1.8V	AG3	GPIO3_D0/I2S0_SCLK
	6	GPIO3_D1/I2S0_LRCK_RX_d_1.8V	I/O	DOWN	I2S0_LRCK_RX	I2S0 port , for audio codec	1.8V	AK1	GPIO3_D1/I2S0_LRCK_RX
	8	GPIO3_D2/I2S0_LRCK_TX_d_1.8V	I/O	DOWN	I2S0_LRCK_TX	I2S0 port , for audio codec	1.8V	AJ2	GPIO3_D2/I2S0_LRCK_TX
	10	GPIO3_D3/I2S0_SDIO_d_1.8V	I/O	DOWN	I2S0_SDIO	I2S0 serial data input 0	1.8V	Y7	GPIO3_D3/I2S0_SDIO
	12	GPIO3_D7/I2S0_SDO0_d_1.8V	I/O	DOWN	I2S0_SDO0	I2S0 serial data output 0	1.8V	AJ1	GPIO3_D7/I2S0_SDO0
	14	GPIO3_D4/I2S0_SD1SD03_d_1.8V	I/O	DOWN	I2S0_SDO3	I2S0 serial data output 3	1.8V	AL1	GPIO3_D4/I2S0_SD1SD03
	16	GPIO3_D5/I2S0_SD1SD02_d_1.8V	I/O	DOWN	I2S0_SDO2	I2S0 serial data output 2	1.8V	AA6	GPIO3_D5/I2S0_SD1SD02
	18	GPIO3_D6/I2S0_SD1SD01_d_1.8V	I/O	DOWN	I2S0_SDO1	I2S0 serial data output 1	1.8V	AH2	GPIO3_D6/I2S0_SD1SD01
	20	GPIO4_A0/I2S_CLK_d_1.8V	I/O	DOWN	I2S_CLK	I2S MCLK, for both I2S0 and I2S1	1.8V	AC7	GPIO4_A0/I2S_CLK
	22	GPIO4_A1/I2C1_SDA_u_1.8V	I/O	UP	I2C1_SDA	I2C serial port 1,for Audio, Core board internal pull up Resistor 2.2K	1.8V	AG1	GPIO4_A1/I2C1_SDA
	24	GPIO4_A2/I2C1_SCL_u_1.8V	I/O	UP	I2C1_SCL	I2C serial port 1,for Audio, Core board internal pull up Resistor 2.2K	1.8V	Y6	GPIO4_A2/I2C1_SCL
	26	GND_17	G		GND	GND			
	28	NC_3							
	30	GND_18	G		GND				
	32	GND_19	G		GND				
	34	GND_20	G		GND				
	36	GND_21	G		GND				
	38	GND_22	G		GND				
	40	GND_23	G		GND				
	42	GPIO2_D3/SDIO0_PWREN_d_1.8V	I/O	DOWN	WIFI_REG_ON_H	WIFI module power enable	1.8V	AD9	GPIO2_D3/SDIO0_PWREN
	44	GPIO0_A3/SDIO0_WRPRT_d_1.8V	I/O	DOWN	WIFI_HOST_WAKE_L	WIFI module wake up AP	1.8V	G39	GPIO0_A3/SDIO0_WRPRT
	46	GPIO2_C6/SDIO0_D2/SP15_CLK_u_1.8V	I/O	UP	SDIO0_D2	SDIO0 data2 port , for WIFI module	1.8V	AG8	GPIO2_C6/SDIO0_D2/SP15_CLK
	48	GPIO2_C7/SDIO0_D3/SP15_CSNO_u_1.8V	I/O	UP	SDIO0_D3	SDIO0 data3 port , for WIFI module	1.8V	AE8	GPIO2_C7/SDIO0_D3/SP15_CSNO
	50	GPIO2_D0/SDIO0_CMD_u_1.8V	I/O	UP	SDIO0_CMD	SDIO0 command output , for WIFI module	1.8V	AF7	GPIO2_D0/SDIO0_CMD
	52	GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1_u_1.8V	I/O	UP	SDIO0_CLK	SDIO0 clock output, for WIFI module	1.8V	AG7	GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1
	54	GPIO2_C4/SDIO0_D0/SP15_RXD_u_1.8V	I/O	UP	SDIO0_D0	SDIO0 data0 port , for WIFI module	1.8V	AD8	GPIO2_C4/SDIO0_D0/SP15_RXD
	56	GPIO2_C5/SDIO0_D1/SP15_TXD_u_1.8V	I/O	UP	SDIO0_D1	SDIO0 data1 port , for WIFI module	1.8V	AK6	GPIO2_C5/SDIO0_D1/SP15_TXD
	58	GND_24	G		GND	GND			
	60	RTC_CLK0_WIFI	I/O	Z	RTC_CLK0_WIFI	32.768K clock output to WIFI , Core board internal pull up Resistor 10K	1.8V	AC32	NPU_GPIO0_C2/CLK10_32K
	62	GPIO2_D4/SDIO0_BKPNR_d_1.8V	I/O	DOWN	BT_REG_ON_H	BT module power enable	1.8V	AF8	GPIO2_D4/SDIO0_BKPNR
	64	GPIO2_C0/UART0_RX_u_1.8V	I/O	UP	UART0_RXD	UART0 serial port, for BT module	1.8V	AE9	GPIO2_C0/UART0_RX
	66	GPIO2_C1/UART0_TX_u_1.8V	I/O	UP	UART0_TXD	UART0 serial port, for BT module	1.8V	AJ6	GPIO2_C1/UART0_TX
	68	GPIO2_C2/UART0_CTSN_u_1.8V	I/O	UP	UART0_CTS	UART0 serial port, for BT module	1.8V	AK7	GPIO2_C2/UART0_CTSN
	70	GPIO2_C3/UART0_RTSN_u_1.8V	I/O	UP	UART0_RTS	UART0 serial port, for BT module	1.8V	AM6	GPIO2_C3/UART0_RTSN
	72	GPIO2_D2/SDIO0_DETIN/PCIE_CLKREQN_u_1.8V	I/O	UP	BT_WAKE_L	AP wake up BT module	1.8V	AJ5	GPIO2_D2/SDIO0_DETIN/PCIE_CLKREQN
	74	GPIO0_A5/EMMC_PWRON_u_1.8V	I/O	UP	BT_HOST_WAKE_L	BT module wake up AP	1.8V	J35	GPIO0_A5/EMMC_PWRON
	76	GND_25	G		GND	GND			
	78	GPIO1_A1/ISPO_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CCO_VCONN_EN_d_1.8V	I/O	DOWN	GPIO1_A1/3G_PWR_EN	3/4G module power enable	1.8V	D39	GPIO1_A1/ISPO_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CCO_VCONN_EN
	80	GPIO4_D5_d_3.0V	I/O	DOWN	TP_INT1	TP_INT input	3.0V	AL2	GPIO4_D5
	82	GPIO2_B3/SP12_CLK/VOP_DEN/CIF_CLKOUTA_u_3.0V	I/O	UP	SP12_CLK/GPI02_B3_u	SP1 bus port 2	3.0V	E34	GPIO2_B3/SP12_CLK/VOP_DEN/CIF_CLKOUTA
	84	GPIO2_B4/SP12_CSNO_u_3.0V	I/O	UP	SP12_CSNO/GPI02_B4_u	SP1 bus port 2	3.0V	E32	GPIO2_B4/SP12_CSNO
	86	GPIO2_B2/SP12_TXD/CIF_CLKIN/I2C6_SCL_u_3.0V	I/O	UP	SP12_TXD/GPI02_B2_u	SP1 bus port 2	3.0V	H26	GPIO2_B2/SP12_TXD/CIF_CLKIN/I2C6_SCL



88	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA_u_3.0V	I/O	UP	SPI2_RXD/GPIO2_B1_u	SPI bus port 2	3.0V	G30	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA
90	GPIO2_A5/VOP_D5/CIF_D5_d_3.0V	I/O	DOWN	SDMMC_PWR	TF CARD power enable	3.0V	G29	GPIO2_A5/VOP_D5/CIF_D5
92	NC_4			NC				
94	GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM_d_3.0V	I/O	DOWN	LCD_BL_PWM0	LCD panel backlight brightness control output	3.0V	AF5	GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM
96	GPIO4_C6/PWM1_d_3.0V	I/O	DOWN	LCD_BL_PWM1	PWM1 output	3.0V	AG6	GPIO4_C6/PWM1
98	GPIO0_A6/PWM3A_IR_d_1.8V	I/O	DOWN	IR_INT	IR receiver input	1.8V	H36	GPIO0_A6/PWM3A_IR
100	GPIO4_C3/UART2C_RX_u_3.0V	I/O	UP	UART2DBG_RX	Uart2 serial port data input, for AP debug	3.0V	AK3	GPIO4_C3/UART2C_RX
102	GPIO4_C4/UART2C_TX_u_3.0V	I/O	UP	UART2DBG_TX	Uart2 serial port data output, for AP debug	3.0V	AJ4	GPIO4_C4/UART2C_TX
104	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA_u_3.0V	I/O	UP	GPIO2_A0/MIPI_PDN0_H	Camera0 power_en (use as I2C2 need external pull-up)	3.0V	D33	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA
106	GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL_u_3.0V	I/O	UP	GPIO2_A1/MIPI_PDN1_H	Camera1 power_en (use as I2C2 need external pull-up)	3.0V	J27	GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL
108	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA_u_3.0V	I/O	UP	EDP_HPD	EDP plug-in detect(use as I2C7 need external pull-up)	3.0V	G32	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA
110	GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL_u_3.0V	I/O	UP	WK2124_INT	WK2124 interrupt input(use as I2C7 need external pull-up)	3.0V	H30	GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL
112	GPIO2_A2/VOP_D2/CIF_D2_d_3.0V	I/O	DOWN	TP_INT	external TP_INT input	3.0V	F33	GPIO2_A2/VOP_D2/CIF_D2
114	GPIO2_A3/VOP_D3/CIF_D3_d_3.0V	I/O	DOWN	AT18_RST	AT18 reset output	3.0V	E33	GPIO2_A3/VOP_D3/CIF_D3
116	GPIO2_A6/VOP_D6/CIF_D6_d_3.0V	I/O	DOWN	WK2124_RST	WK2124 reset output	3.0V	H29	GPIO2_A6/VOP_D6/CIF_D6
118	GPIO3_B2/MAC_RXER/I2C5_SDA_u_3.3V	I/O	UP	LCD_RST	LCD reset output	3.0V	F23	GPIO3_B2/MAC_RXER/I2C5_SDA
120	GPIO2_A4/VOP_D4/CIF_D4_d_3.0V	I/O	DOWN	PCIE_RST	PCIE reset output	3.0V	G33	GPIO2_A4/VOP_D4/CIF_D4
122	NC_5			NC				
124	GND_26	G		GND				
126	MIPI_TX0_D3P	0		MIPI_TX0_D3P	MIPI-DSIO differential lane 3 positive		AP6	MIPI_TX0_D3P
128	MIPI_TX0_D3N	0		MIPI_TX0_D3N	MIPI-DSIO differential lane 3 negative		AP5	MIPI_TX0_D3N
130	MIPI_TX0_D2P	0		MIPI_TX0_D2P	MIPI-DSIO differential lane 2 positive		AT4	MIPI_TX0_D2P
132	MIPI_TX0_D2N	0		MIPI_TX0_D2N	MIPI-DSIO differential lane 2 negative		AK5	MIPI_TX0_D2N
134	MIPI_TX0_CLKP	0		MIPI_TX0_CLKP	MIPI-DSIO differential clock lane positive		AT6	MIPI_TX0_CLKP
136	MIPI_TX0_CLKN	0		MIPI_TX0_CLKN	MIPI-DSIO differential clock lane negative		AU5	MIPI_TX0_CLKN
138	MIPI_TX0_D1P	0		MIPI_TX0_D1P	MIPI-DSIO differential lane 1 positive		AT8	MIPI_TX0_D1P
140	MIPI_TX0_D1N	0		MIPI_TX0_D1N	MIPI-DSIO differential lane 1 negativ		AU8	MIPI_TX0_D1N
142	MIPI_TX0_D0P	0		MIPI_TX0_D0P	MIPI-DSIO differential lane 0 positive		AT9	MIPI_TX0_D0P
144	MIPI_TX0_D0N	0		MIPI_TX0_D0N	MIPI-DSIO differential lane 0 negativ		AU9	MIPI_TX0_D0N
146	GND_27	G		GND				
148	ADC_IN0	A		ADC_IN0	ADC input ,Core board internal pull up Resistor 10K	1.8V	W27	ADC_IN0
150	ADC_IN1	A		ADC_IN1	ADC input ,Core board internal pull up Resistor 10K	1.8V	Y29	ADC_IN1
152	ADC_IN2	A		RECOVER	ADC RECOVER_KEY input , Core board internal pull up Resistor 10K	1.8V	Y28	ADC_IN2
154	ADC_IN3	A		LINE_IN_DET	ADC input(Line_IN plug in detect) , Core board internal pull up Resistor 10K	1.8V	Y27	ADC_IN3
156	ADC_IN4	A		HP_DET	ADC input , Core board internal pull up Resistor 10K	1.8V	AA28	ADC_IN4
158	GPIO0_B0/SDMMC_WRP1/TEST_CLKOUT2_u_1.8V	I/O	UP	PCIE_WAKE	AP wake up PCIE	1.8V	F39	GPIO0_B0/SDMMC_WRP1/TEST_CLKOUT2
160	GPIO4_D0/PCIE_CLKREQNB_u_3.0V	I/O	UP	PCIE_CLKREQ	PCIE_CLKREQN	3.0V	AJ3	GPIO4_D0/PCIE_CLKREQNB
162	GPIO0_B4/TCPD_VBUS_BDIS_d_1.8V	I/O	DOWN	GPIO0_B4	PCIE Reset	1.8V	J37	GPIO0_B4/TCPD_VBUS_BDIS
164	GND_28	G		GND				
166	GPIO4_B1/SDMMC_D1/UART2A_TX_u_3.3V	I/O	UP	SDMMC_D1	SDMMC_D1 data port,for TF Card		P31	GPIO4_B1/SDMMC_D1/UART2A_TX
168	GPIO4_B0/SDMMC_D0/UART2A_RX_u_3.3V	I/O	UP	SDMMC_D0	SDMMC_D0 data port, for TF Card		P32	GPIO4_B0/SDMMC_D0/UART2A_RX
170	GPIO4_B2/SDMMC_D2/APJTAG_TCK_u_3.3V	I/O	UP	SDMMC_D2	SDMMC_D2 data port, for TF Card		M34	GPIO4_B2/SDMMC_D2/APJTAG_TCK
172	GPIO4_B5/SDMMC_CMD/MCUJTAG_TMS_u_3.3V	I/O	UP	SDMMC_CMD	SDMMC command output,for TF Card		H40	GPIO4_B5/SDMMC_CMD/MCUJTAG_TMS
174	GPIO4_B3/SDMMC_D3/APJTAG_TMS_u_3.3V	I/O	UP	SDMMC_D3	SDMMC_D3 data port, for TF Card		H39	GPIO4_B3/SDMMC_D3/APJTAG_TMS
176	GPIO4_B4/SDMMC_CLKOUT/MUCJTAG_TCK_d_3.3V	I/O	DOWN	SDMMC_CLK	SDMMC clock output,for TF Card , Core board internal series resistance 22R		G40	GPIO4_B4/SDMMC_CLKOUT/MUCJTAG_TCK
<b>Note 2: Default is 3.3V; SDMMC0 1.8V(SDIO3.0 model)/3.0V(SDIO2.0 model) Auto</b>								
178	GPIO0_A7/SDMMC_DET_u_1.8V	I/O	UP	SDMMC_DET	Sdmmc card detect signal, 0: TF card insert 1: TF card no insert	1.8V	M35	GPIO0_A7/SDMMC_DET
180	GND_29	G						
182	GPIO3_B5/MAC_MDIO/UART1_TX_u_3.3V	I/O	UP	MAC_MDIO	MAC management command and data	3.3V	G26	GPIO3_B5/MAC_MDIO/UART1_TX
184	GPIO3_B3/MAC_CLK/I2C5_SCL_u_3.3V	I/O	UP	MAC_MDC	MAC management clock	3.3V	F30	GPIO3_B0/MAC_MDC/SPI0_CS_N1
186	GPIO3_B0/MAC_MDC/SPI0_CS_N1_u_3.3V	I/O	UP	PHY_TXCLK	MAC transmit clock , Core board internal series resistance 22R	3.3V	G27	GPIO3_C1/MAC_TXCLK/UART3_RTSN
188	GPIO3_B6/MAC_RXCLK/UART3_RX_u_3.3V	I/O	UP	MAC_RXCLK	MAC receive clock	3.3V	F26	GPIO3_B6/MAC_RXCLK/UART3_RX
190	GND_30	G		GND				



192	GPIO3_C1/MAC_TXCLK/UART3_RTSN_u_3.3V	I/O	UP	MAC_CLK	MAC reference clock output , I2C serial port 5, need external pull-up , Core board internal series resistance 0R	3.3V	G24	GPIO3_B3/MAC_CLK/I2C5_SCL
194	GPIO3_A7/MAC_RXD1/SPI0_CSNO_u_3.3V	I/O	UP	MAC_RXD1	MAC receive data	3.3V	H27	GPIO3_A7/MAC_RXD1/SPI0_CSNO
196	GPIO3_A3/MAC_RXD3/SPI4_CSNO_u_3.3V	I/O	UP	MAC_RXD3	MAC receive data	3.3V	E26	GPIO3_A3/MAC_RXD3/SPI4_CSNO
198	GPIO3_A6/MAC_RXD0/SPI0_CLK_u_3.3V	I/O	UP	MAC_RXD0	MAC receive data	3.3V	F27	GPIO3_A6/MAC_RXD0/SPI0_CLK
200	GPIO3_A2/MAC_RXD2/SPI4_CLK_u_3.3V	I/O	UP	MAC_RXD2	MAC receive data	3.3V	F29	GPIO3_A2/MAC_RXD2/SPI4_CLK
202	GPIO3_B1/MAC_RXDV_d_3.3V	I/O	DOWN	MAC_RXDV	MAC receive data valid	3.3V	E27	GPIO3_B1/MAC_RXDV
204	GPIO3_A4/MAC_TXD0/SPI0_RXD_d_3.3V	I/O	DOWN	PHY_TXD0	MAC transmit data , Core board internal series resistance 22R	3.3V	D26	GPIO3_A4/MAC_TXD0/SPI0_RXD
206	GPIO3_A0/MAC_TXD2/SPI4_RXD_d_3.3V	I/O	DOWN	PHY_TXD2	MAC transmit data , Core board internal series resistance 22R	3.3V	F24	GPIO3_A0/MAC_TXD2/SPI4_RXD
208	GPIO3_A1/MAC_TXD3/SPI4_TXD_d_3.3V	I/O	DOWN	PHY_TXD3	MAC transmit data , Core board internal series resistance 22R	3.3V	H24	GPIO3_A1/MAC_TXD3/SPI4_TXD
210	GPIO3_A5/MAC_TXD1/SPI0_TXD_d_3.3V	I/O	DOWN	PHY_TXD1	MAC transmit data , Core board internal series resistance 22R	3.3V	G23	GPIO3_A5/MAC_TXD1/SPI0_TXD
212	GPIO3_B4/MAC_TXEN/UART1_RX_u_3.3V	I/O	UP	PHY_TXEN	MAC transmit enable	3.3V	H23	GPIO3_B4/MAC_TXEN/UART1_RX
214	GPIO3_C0/MAC_COL/UART3_CTSN/SPDIF_TX_u_3.3V	I/O	UP	FAN_CTL	PHY interrupt input, I2C serial port 5, need external pull-up	3.3V	E29	GPIO3_C0/MAC_COL/UART3_CTSN/SPDIF_TX
216	GPIO3_B7/MAC_CRS/UART3_TX/CIF_CLKOUTB_u_3.3V	I/O	UP	PHY_RST	MAC carrier sense detect	3.3V	E30	GPIO3_B7/MAC_CRS/UART3_TX/CIF_CLKOUTB
218	NPOR	I	UP	RESET_KEY	system reset signal Input. External connection Reset key, active low			NPOR
220	EXT_EN_H	O		PMIC_EXT_EN	External Power enable output, Voltage 5V			
222	GND_31	G		GND	GND			
224	VCC_1V8_S3	P		VDD10_WL(LDO)	Output Voltage 1.8V, MAX output current 200mA			
226	VCCIO_3V3_S0	P		VCC_LAN(DCDC)	Output Voltage 3.3V, MAX output current 500mA			
228	VCCA1V8_CODEC_2	P		VCCA1V8_CODEC(LDO)	Output Voltage 1.8V, MAX output current 200mA			
230	VCCIO_3V0_S0_2	P		VCCA3V0_CODEC(LDO)	Output Voltage 3.0V, MAX output current 200mA			
232	VCC_RTC	P		VCC_RTC	Input Voltage 3.3V-5.5V , MAX input current 50mA			
234	VCC3V3_SYS_2	P		VCC3V3_SYS(DCDC)	Output Voltage 3.3V, MAX output current 500mA			
236	SPKP_OUT	O		TP3	Positive speaker driver output. (not connect)			
238	SPKN_OUT	O		TP4	Negative speaker driver output. (not connect)			
240	HPL	O		HPL	Left channel output of the headphone			
242	HPR	O		HPR	Right channel output of the headphone			
244	GND_32	G		Power ground	Power ground  System Power supply Input Voltage : Min 4.8V, Typ 5.0V, Max 5.2V Input current: Typ 1000mA ;Max 2200mA			
246	GND_33	G		Power ground				
248	GND_34	G		Power ground				
250	GND_35	G		Power ground				
252	VCC_SYS_2	P		VCC5V0_SYS				
254	VCC_SYS_4	P		VCC5V0_SYS				
256	VCC_SYS_6	P		VCC5V0_SYS				
258	VCC_SYS_8	P		VCC5V0_SYS				
260	VCC_SYS_10	P		VCC5V0_SYS				

## 关于我们

### 公司简介

天启科技成立于 2009 年，国家高新技术企业，专注于开源智能硬件，人工智能，物联网，数字音频产品的研发设计、生产和销售，同时提供了智能软硬件产品的整体解决方案。开源品牌“Firefly”在互联网上拥有开源社区与网上商城，目前已超过 20 万用户与 10000 多家的企业用户，为众多科技创业者与初创企业加速研发进程，并提供专业的技术服务。

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