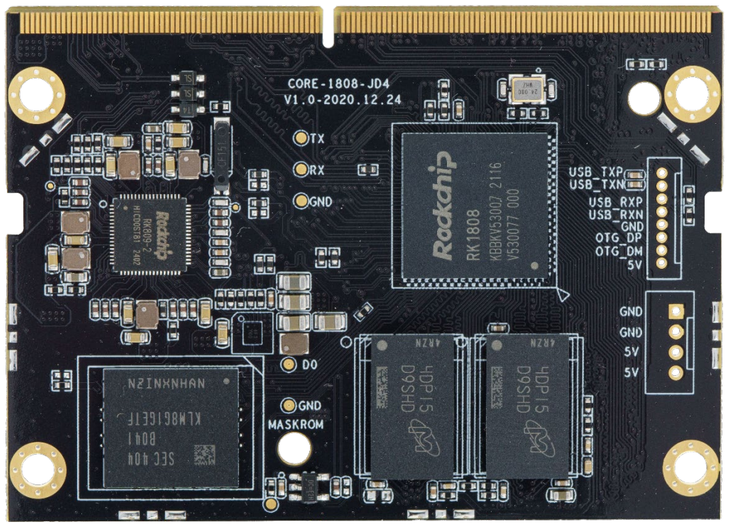
Core-1808-JD4

AI Core board



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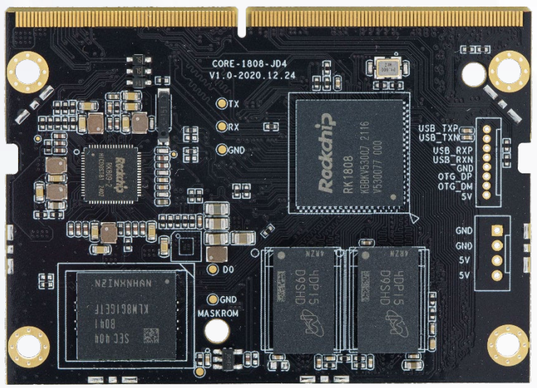
T-CHIP INTELLIGENCE TECHNOLOGY

Product features



Dual-core 64-bit AI processor RK1808

The core board is equipped with Rockchip RK1808 AI chip, and the CPU adopts dual core 64 bit Cortex-A35 architecture, with a maximum clock speed of 1.6GHz.

Powerful AI computing capabilities

The inbuilt NPU has a calculation capacity up to 3TOPS, supports INT8/INT16/FP16 mixed operation, and coordinates performance, power consumption and operational precision to the greatest extent. It also supports the network model conversion of frameworks like TensorFlow, Caffe, ONNX and Darknet.

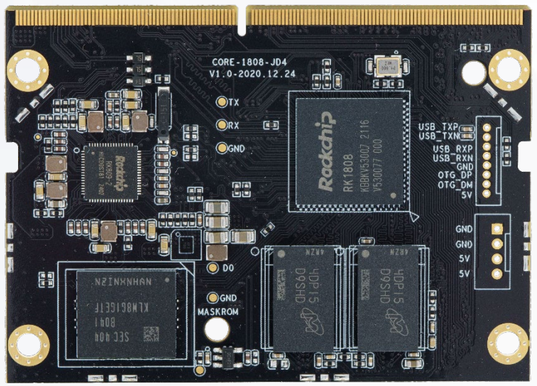
A variety of display interfaces

Support single MIPI-DSI, 1080P@60fps output; Support RGB interface; It has a 2MP ISP image signal processor and supports dual camera function.

Strong network communication capabilities

Integrated GMAC Ethernet Manager, providing RGMII/RMII interface, expandable 1 Gigabit Ethernet; WiFi and Bluetooth can be expanded via SDIO3.0.

Product features



Support Linux operating system

It supports Linux+QT operating system, provides a safe and stable system environment for product research and production, and meets the application needs of different scenarios.

Stable and reliable

Adopts SODIMM 260P interface which brings the data transmission and extension performance into full play. Through the immersive craft, it is corrosion-resistant, solid and reliable.

Rich extension interfaces

Equipped with MIPI-CSI, MIPI-DSI, DVP, PCIe 2.1, USB 3.0, USB 2.0, SDIO, I2C, I2S, SPI, UART, PWM, GPIO and other extension interfaces, it is convenient to connect various peripherals.

Wide range of application scenarios

Widely used in scenarios such as voice wake-up, speech recognition, face detection and attribute analysis, face recognition, pose analysis, object detection and recognition, image processing, etc.

Specifications

Specifications		
Basic Specifications	SOC	Rockchip RK1808
	CPU	Dual-core 64-bit processor Cortex-A35, main frequency up to 1.6GHz
	NPU	Peak computing power up to 3 TOPS, supports OpenCL/OpenVX, and supports INT8/INT16/FP16 hybrid computing Support network model conversion using frameworks such as TensorFlow, Caffe, ONNX, Darknet, etc.
	ISP	Support 2MP, AE/AWB/AF/Hist
	Codecs	Video Decoding: 1080P@60fps H.264/AVC Video Encoding: 1080P@30fps H.264
	RAM	1GB DDR3 (1GB/2GB/4GB optional)
	Storage	8GB High-speed eMMC4.51(8GB/16GB/32GB/128GB optional) Supports TF card expansion and PCIe 2.1
	OS	Linux+Qt
	Power	5V (voltage tolerance ± 5%)
	Power consumption	Normal: 1.25W (5V/250mA), Max: 2.15W (5V/430mA)
	Interface	Goldfinger (260 PIN, SODIMM, 0.5mm pitch)
	Size	69.6mm × 50.0mm × 8.2mm
	Environment	Operating Temperature: -20℃ ~ 60℃, Storage Temperature: -20℃ ~ 70℃, Storage Humidity: 10% ~ 90%RH(non-condensing)
Interface Specifications	Internet	1 × GMAC, RGMII/RMII interface, support 10/100/1000Mbps data transfer rate, WiFi and Bluetooth can be expanded through SDIO3.0
	Video input	1 × MIPI-CSI Camera Interface (Built-in Dual Hardware ISP, supports single 13Mpixel or dual 8Mpixel) 1 × DVP
	Video output	1 × MIPI-DSI (Supports single-channel 1080P@60fps output) 1 × RGB (18-bit(RGB666), maximum support 1280×800@60fps)
	Audio	1 × I2S (Used for audio input and output) 1 × 3.5mm audio jack (left and right channels) 2 × MIC Mono Speaker(8Ω, 1.3W)
	USB	1 × USB3.0(Multiplexed with PCIe 2.1), 1 × USB2.0 HOST, 1 × USB2.0 OTG
	Other interfaces	Built in 1-ch&8-ch I2S&8-ch PDM, built-in VAD 7 × UART, 3 × SPI, 5 × I2C, 10 × PWM, 4 × SARADC, I2S, GPIOs

Interface description

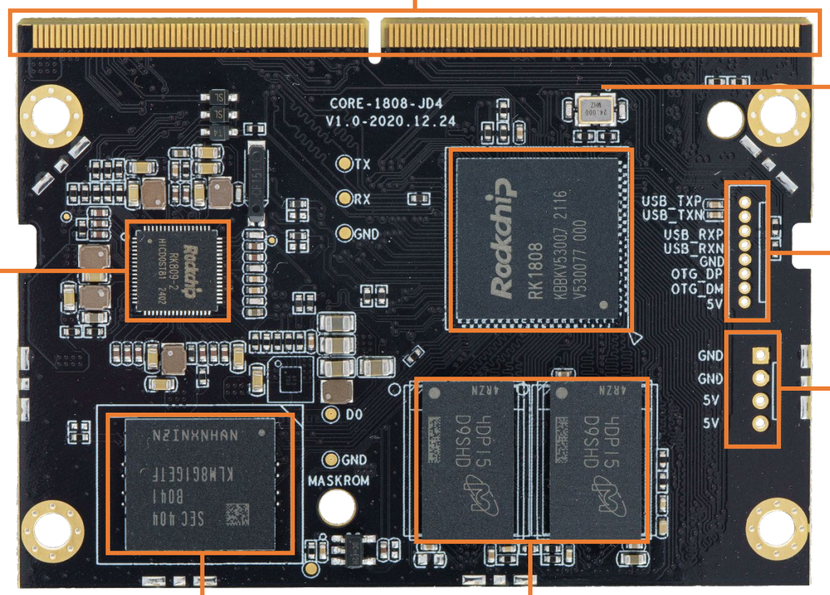
Goldfinger
(SODIMM, 260Pin, 0.5mm pitch)

Rockchip RK1808
(Main frequency is up to 1.6GHz)

PMU
(Power Management Unit)

USB3.0

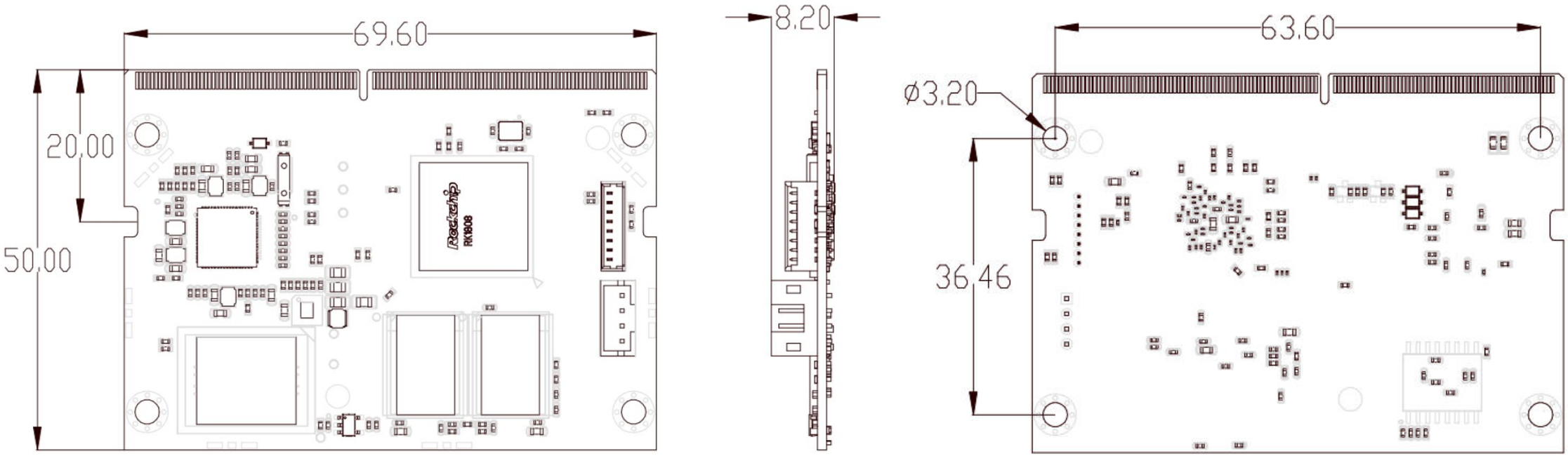
Power input/output



eMMC
(8GB/16GB/32GB/128GB optional)

DDR3
(1GB/2GB/4GB optional)

Dimension



Interface definition

Notes1:
① : Pad types: I = input, O = output, I/O = input/output (bidirectional), G= Ground ,
P = power supply , DOWN = Internal pull down , UP = Internal pull UP L = Lowe Level H = High level”

pin	Core board pin definition	Pad type	IO Pull	Reset State	function for Floor	Default function description	IO Power domain	RK1808 Pin Number	RK1808 Pin Name
1	GND_1	G		GND	GND	GND	GND		GND_1
3	GPIO0_B4/UART0_CTS_u_3.3V	I/O	UP	I/GPIO	WORK_LED	System LED control 1:Enable 0:Disable	3.3V	AR15	GPIO0_B4/UART0_CTS
5	GPIO0_B5/UART0_RTS/TEST_CLK1_u_3.3V	I/O	UP	I/GPIO	DIY _LED	Diy led control 1:Enable 0:Disable	3.3V	AV10	GPIO0_B5/UART0_RTS/TEST_CLK1
7	GPIO0_B2/UART0_TX_d_3.3V	I/O	DOWN	I/GPIO	VCC5V0_HOST_EN	Host usb 5v power enable 1:Enable 0:Disable	3.3V	AU15	GPIO0_B2/UART0_TX
9	GPIO0_B3/UART0_RX_d_3.3V	I/O	DOWN	I/GPIO	VCC5V0_OTG_EN	OTG 5v power enable 1:Enable 0:Disable	3.3V	AW9	GPIO0_B3/UART0_RX
11	GPIO2_C7/LCDC_DEN_d_3.3V	I/O	DOWN	I/GPIO	LVDS_RESX	LVDS Reset	3.3V	AV34	GPIO2_C7/LCDC_DEN
13	GPIO0_C0/I2C1_SCL_d_3.3V	I/O	DOWN	I/GPIO	I2C1_SCL	I2C clock , Core board interiorl pull up Resistor 2.2K	3.3V	AN13	GPIO0_C0/I2C1_SCL
15	GPIO0_C1/I2C1_SDA_d_3.3V	I/O	DOWN	I/GPIO	I2C1_SDA	I2C data ， Core board interiorl pull up Resistor 2.2K	3.3V	AV12	GPIO0_C1/I2C1_SDA
17	GPIO3_C2/LCDC_D8/UART5_TX/I2C4_SCL_d_3.3V	I/O	DOWN	I/GPIO	LCD_EN	Lcd enable ， Core board interiorl pull up Resistor 2.2K	3.3V	AN37	GPIO3_C2/LCDC_D8/UART5_TX/I2C4_SCL
19	GPIO3_C3/LCDC_D9/UART5_RX/I2C4_SDA_d_3.3V	I/O	DOWN	I/GPIO	CAM_PWR	Camera power enable ， Core board interiorl pull up Resistor 2.2K	3.3V	AM38	GPIO3_C3/LCDC_D9/UART5_RX/I2C4_SDA
21	GPIO2_B1/CIF_D7/RGMII_COL_d_1.8V	I/O	DOWN	I/GPIO	MIPI_PWR_EN	MIPI power enable , Core board internal pull-down resistor 12K, parallel 10K	1.8V	AW27	GPIO2_B1/CIF_D7/RGMII_COL
23	NC_1								
25	GPIO0_A0/REF_CLKO_d_1.8V	I/O	DOWN	I/GPIO	MIPI_RST	Mipi reset	1.8V	AV22	GPIO0_A0/REF_CLKO

Interface definition

27	GPIO0_A7/PCIE_WAKE_M0_u_1.8V	I/O	UP	I/GPIO	LCD_BL_EN	LCD panel power enable	1.8V	AR21	GPIO0_A7/PCIE_WAKE_M0
29	GPIO1_B6/SPI0_CSN_u_3.3V	I/O	UP	I/GPIO	GPIO1_B6/SPI0_CSN	SPI bus port 1， Core board interiorl pull up Resistor 10K	3.3V	G25	GPIO1_B6/SPI0_CSN
31	NC_67								
33	NC_68								
35	GPIO1_B7/SPI0_CLK/PWM5_d_3.3V	I/O	DOWN	I/GPIO	SPI0_CLK/PWM5/GPIO1_B7	SPI serial clock	3.3V	E25	GPIO1_B7/SPI0_CLK/PWM5
37	GPIO3_C6/LCDC_D12/UART7_TX_d_3.3V	I/O	DOWN	I/GPIO	TP_RST	Tp reset	3.3V	AN39	GPIO3_C6/LCDC_D12/UART7_TX
39	NC_69								
41	GPIO3_D3/LCDC_D17/PWM11/SPI1_CSN1_M1_d_3.3V	I/O	DOWN	I/GPIO	SPK_CTL_H	Control play and stop of spk	3.3V	AJ37	GPIO3_D3/LCDC_D17/PWM11/SPI1_CSN1_M1
43	GND_2	G		GND	GND	GND	GND		GND_2
45	NC_2								
47	NC_3								
49	NC_4								
51	NC_5								
53	NC_6								
55	NC_7								
57	NC_8								
59	NC_9								
61	NC_10								

Interface definition

63	NC_11								
65	GND_3	G		GND	GND	GND	GND		GND_3
67	DPHY_RX_D3P	A			MIPI_RX0_D3P	MIPI-CSI0 differential lane 3 positive	1.8V	T38	DPHY_RX_D3P
69	DPHY_RX_D3N	A			MIPI_RX0_D3N	MIPI-CSI0 differential lane 3 positive	1.8V	R39	DPHY_RX_D3N
71	DPHY_RX_D2P	A			MIPI_RX0_D2P	MIPI-CSI0 differential lane 2 positive	1.8V	P38	DPHY_RX_D2P
73	DPHY_RX_D2N	A			MIPI_RX0_D2N	MIPI-CSI0 differential lane 2 negative	1.8V	N39	DPHY_RX_D2N
75	DPHY_RX_CLKP	A			MIPI_RX0_CLKP	MIPI-CSI0 differential clock lane positive	1.8V	M38	DPHY_RX_CLKP
77	DPHY_RX_CLKN	A			MIPI_RX0_CLKN	MIPI-CSI0 differential clock lane negative	1.8V	L39	DPHY_RX_CLKN
79	DPHY_RX_D1P	A			MIPI_RX0_D1P	MIPI-CSI0 differential lane 1 positive	1.8V	K38	DPHY_RX_D1P
81	DPHY_RX_D1N	A			MIPI_RX0_D1N	MIPI-CSI0 differential lane 1 negative	1.8V	J39	DPHY_RX_D1N
83	DPHY_RX_D0P	A			MIPI_RX0_D0P	MIPI-CSI0 differential lane 0 positive	1.8V	N35	DPHY_RX_D0P
85	DPHY_RX_D0N	A			MIPI_RX0_D0N	MIPI-CSI0 differential lane 0 negative	1.8V	L35	DPHY_RX_D0N
87	GND_4	G		GND	GND	GND	GND		GND_4
89	NC_12								
91	NC_13								
93	NC_14								
95	NC_15								
97	GND_5	G		GND	GND	GND	GND		GND_5

Interface definition

99	NC_16								
101	NC_17								
103	NC_18								
105	NC_19								
107	NC_20								
109	NC_21								
111	NC_22								
113	NC_23								
115	GND_6	G		GND	GND	GND	GND		GND_6
117	USB_OTG_ID_3.3V	A			USB_OTG_ID	OTG Role switching Input (no used) 0: HOST Mode 1: Slave Mode	3.3V	AJ9	USB_OTG_ID
119	NC_24								
121	NC_25								
123	NC_26								
125	PCIE_RX0N/USB3_SSRXN	A			USB3_SSRXN	Channel 0 negative serial input	1.8V	AP2	PCIE_RX0N/USB3_SSRXN
127	PCIE_RX0P/USB3_SSRXP	A			USB3_SSRXP	Channel 0 positive serial input	1.8V	AR1	PCIE_RX0P/USB3_SSRXP
129	PCIE_TX0P/USB3_SSTXP	A			USB3_SSTXP	Channel 0 positive serial output	1.8V	AU1	PCIE_TX0P/USB3_SSTXP
131	PCIE_TX0N/USB3_SSTXN	A			USB3_SSTXN	Channel 0 negative serial output	1.8V	AT2	PCIE_TX0N/USB3_SSTXN
133	USB_OTG_DP	A			USB_OTG_DP	OTG_DP	3.3V	AL1	USB_OTG_DP

Interface definition

135	USB_OTG_DM	A			USB_OTG_DM	OTG_DM	3.3V	AK2	USB_OTG_DM
137	NC_27								
139	NC_28								
141	NC_29								
143	NC_30								
145	USB_OTG_VBUS	A			VBUS_DET	Vbus power detect for USB3.0， Core board interiorl pull up Resistor 10K	3.3V	AL9	USB_OTG_VBUS
147	GND_7	G			GND	GND	GND		GND_7
149	NC_31								
151	NC_32								
153	NC_33								
155	NC_34								
157	NC_35								
159	NC_36								
161	NC_37								
163	NC_38								
165	PCIE_RX1P	A			PCIE_RX1_P	Channel 1 positive serial input	1.8V	AW3	PCIE_RX1P
167	PCIE_RX1N	A			PCIE_RX1_N	Channel 1 negative serial input	1.8V	AV4	PCIE_RX1N
169	PCIE_TX1P	A			PCIE_TX1P	Channel 1 positive serial output	1.8V	AR5	PCIE_TX1P

Interface definition

171	PCIE_TX1N	A			PCIE_TX1N	Channel 1 negative serial output	1.8V	AR7	PCIE_TX1N
173	NC_39								
175	NC_40								
177	NC_41								
179	NC_42								
181	PCIE_REFCLKN	A			PCIE_REF_CLKN	Low-swing differential clock pair	1.8V	AN7	PCIE_REFCLKN
183	PCIE_REFCLKP	A			PCIE_REF_CLKP	Low-swing differential clock pair	1.8V	AN5	PCIE_REFCLKP
185	GND_8	G			GND	GND	GND		GND_8
187	USB_HOST_DP	A			HOST0_DP	USB 2.0 Data signal DP	3.3V	AN1	USB_HOST_DP
189	USB_HOST_DM	A			HOST0_DM	USB 2.0 Data signal DM	3.3V	AM2	USB_HOST_DM
191	GND_9	G			GND	GND	GND		GND_9
193	NC_43								
195	NC_44								
197	GND_10	G			GND	GND	GND		GND_10
199	NC_45								
201	NC_46								
203	NC_47								
205	NC_48								

Interface definition

207	NC_49								
209	NC_50								
211	NC_51								
213	NC_52								
215	NC_53								
217	NC_54								
219	GND_11	G			GND	GND	GND		GND_11
221	POWER_ON				POWER_ON	Power on Signal Input, External connection Power key , active low	To POWER_KEY		
223	NC_55								
225	VDDIO_WL_1	P			VDDIO_WL (LDO)	Output Voltage 1.8V,Rated output current 300mA	1.8V		
227	VCC_3V3_S0_1	P			VCC_LAN (LDO)	(VCCIO_3V3) Output Voltage 3.3V,Rated output current 500mA	3.3V		
229	VCCA1V8_CODEC_1	P			VCCA1V8_CODEC (LDO)	Output Voltage 1.8V,Rated output current 300mA	1.8V		
231	VCCA3V0_CODEC_1	P			VCCA3V0_CODEC (LDO)	Output Voltage 3.0V,Rated output current 100mA	3.0V		
233	VCC_5V_S	P			VCC_5V_S	Input Voltage 3.3V-5.5V, Rated input current 50mA	5.0V		
235	VCC3V3_SYS_1	P			VCC_3V3 (DCDC)	Output Voltage 3.3V,Rated output current 1A	3.3V		
237	HP_SNS				HP_SNS	Reference ground for the headphone			
239	MIC2_IN				MIC2_IN	Negative input of the Microphone			
241	MIC1_IN				MIC1_IN	Positive input of the Microphone			

Interface definition

243	GND_12	G			GND	Power ground	GND		GND_12
245	GND_13	G			GND		GND		GND_13
247	GND_14	G			GND		GND		GND_14
249	GND_15	G			GND		GND		GND_15
251	VCC5V0_SYS_1	P			VCC5V0_SYS	System Power supply Input Voltag : Min 4.8V,Typ 5.0V, Max 5.2V Input current: Typ 400mA ;Max 700mA	5.0V		
253	VCC5V0_SYS_2	P			VCC5V0_SYS		5.0V		
255	VCC5V0_SYS_3	P			VCC5V0_SYS		5.0V		
257	VCC5V0_SYS_4	P			VCC5V0_SYS		5.0V		
259	VCC5V0_SYS_12	P			VCC5V0_SYS		5.0V		

pin	Core board pin definition	Pad type	IO Pull	Reset State	function for Floor	Default function description	IO Power domain	RK1808 Pin Number	RK1808 Pin Name
2	GND_16	G			GND	GND	GND		GND_16
4	GPIO3_B7/I2S0_SCLK_TX/ISP_PRELIGHTTRIG_d_3.0V	I/O	DOWN	I/GPIO	I2S0_SCLK_TX	I2S 0 port, for audio codec	3.0V	AD38	GPIO3_B7/I2S0_SCLK_TX/ISP_PRELIGHTTRIG
6	GPIO3_B1/I2S0_LRCK_RX/PDM_CLK1_d_3.0V	I/O	DOWN	I/GPIO	I2S0_LRCK_RX	I2S 0 port, for audio codec	3.0V	AB38	GPIO3_B1/I2S0_LRCK_RX/PDM_CLK1
8	GPIO3_B6/I2S0_LRCK_TX/ISP_FLASHTRIGOUT_d_3.0V	I/O	DOWN	I/GPIO	I2S0_LRCK_TX	I2S 0 port, for audio codec	3.0V	AE39	GPIO3_B6/I2S0_LRCK_TX/ISP_FLASHTRIGOUT
10	GPIO3_C1/I2S0_SDI0/PDM_SDI0_d_3.0V	I/O	DOWN	I/GPIO	I2S0_SDI0	I2S 0 port, for audio codec	3.0V	AA39	GPIO3_C1/I2S0_SDI0/PDM_SDI0
12	GPIO3_C0/I2S0_SDO0/ISP_SHUTTERTRIG_d_3.0V	I/O	DOWN	I/GPIO	I2S0_SDO0	I2S 0 port, for audio codec	3.0V	AC37	GPIO3_C0/I2S0_SDO0/ISP_SHUTTERTRIG
14	GPIO3_B2/I2S0_SDO3/ISP_FLASHTRIGIN/LCDC_HSYNC_M1_d_3.0V	I/O	DOWN	I/GPIO	I2S0_SDO3	I2S 0 port, for audio codec	3.0V	AC33	GPIO3_B2/I2S0_SDO3/ISP_FLASHTRIGIN/LCDC_HSYNC_M1
16	GPIO3_B3/I2S0_SDO2/I2C2_SCL_M0/LCDC_VSYNC_M1_d_3.0V	I/O	DOWN	I/GPIO	I2S0_SDO2	I2S 0 port, for audio codec	3.0V	AC31	GPIO3_B3/I2S0_SDO2/I2C2_SCL_M0/LCDC_VSYNC_M1

Interface definition

18	GPIO3_B4/I2S0_SDO1/I2C2_SDA_M0_d_3.0V	I/O	DOWN	I/GPIO	I2S0_SDO1	I2S 0 port, for audio codec	3.0V	AC35	GPIO3_B4/I2S0_SDO1/I2C2_SDA_M0
20	GPIO3_B5/I2S0_MCLK/ISP_SHUTTEREN_d_3.0V	I/O	DOWN	I/GPIO	I2S_CLK	I2S MCLK, for both I2S0 and I2S1	3.0V	AC39	GPIO3_B5/I2S0_MCLK/ISP_SHUTTEREN
22	GPIO2_D1/I2C3_SDA/UART2_RX_M1_u_3.3V	I/O	UP	I/GPIO	I2C3_SDA	I2C serial port 1,for Audio, Core board interiorl pull up Resistor 2.2K	3.3V	AV36	GPIO2_D1/I2C3_SDA/UART2_RX_M1
24	GPIO2_D0/I2C3_SCL/UART2_TX_M1_u_3.3V	I/O	UP	I/GPIO	I2C3_SCL	I2C serial port 1,for Audio, Core board interiorl pull up Resistor 2.2K	3.3V	AW37	GPIO2_D0/I2C3_SCL/UART2_TX_M1
26	GND_17	G			GND	GND	GND		GND_17
28	NC_56								
30	GPIO3_B0/I2S0_SCLK_RX/PDM_CLK0_d_3.0V	I/O	DOWN		I2S0_SCLK_RX	I2S serial clock	3.0V	Y38	GPIO3_B0/I2S0_SCLK_RX/PDM_CLK0
32	GPIO3_A7/I2S0_SDI1/PDM_SDI1_d_3.0V	I/O	DOWN		I2S0_SDI1	I2S serial data input	3.0V	AC29	GPIO3_A7/I2S0_SDI1/PDM_SDI1
34	GPIO3_A5/I2S0_SDI3/PDM_SDI3_d_3.0V	I/O	DOWN		I2S0_SDI3	I2S serial data input	3.0V	AA31	GPIO3_A5/I2S0_SDI3/PDM_SDI3
36	GPIO3_A6/I2S0_SDI2/PDM_SDI2_d_3.0V	I/O	DOWN		I2S0_SDI2	I2S serial data input	3.0V	W35	GPIO3_A6/I2S0_SDI2/PDM_SDI2
38	NC_57								
40	GND_18	G			GND	GND	GND		GND_18
42	GPIO4_C0/SPI1_CSN1_M0_u_1.8V	I/O	UP		WIFI_REG_ON_H	WIFI module power enable	1.8V	AL33	GPIO4_C0/SPI1_CSN1_M0
44	GPIO4_C1/I2C5_SCL_u_1.8V	I/O	UP		WIFI_HOST_WAKE_L	WIFI module wake up AP	1.8V	AR39	GPIO4_C1/I2C5_SCL
46	GPIO4_B2/SDMMC1_D2/UART1_CTS_u_1.8V	I/O	UP		SDIO0_D2	SDIO1 data port , for WIFI module	1.8V	AT38	GPIO4_B2/SDMMC1_D2/UART1_CTS
48	GPIO4_B3/SDMMC1_D3/UART1_RTS_u_1.8V	I/O	UP		SDIO0_D3	SDIO1 data port , for WIFI module	1.8V	AP38	GPIO4_B3/SDMMC1_D3/UART1_RTS
50	GPIO4_A6/SDMMC1_CMD_u_1.8V	I/O	UP		SDIO0_CMD	SDIO0 command output , for WIFI module	1.8V	AR31	GPIO4_A6/SDMMC1_CMD
52	GPIO4_A7/SDMMC1_CLK_d_1.8V	I/O	DOWN		SDIO0_CLK	SDIO0 clock output, for WIFI module	1.8V	AR35	GPIO4_A7/SDMMC1_CLK

Interface definition

54	GPIO4_B0/SDMMC1_D0/UART1_RX_M0_u_1.8V	I/O	UP		SDIO0_D0	SDIO0 data port , for WIFI module	1.8V	AN31	GPIO4_B0/SDMMC1_D0/UART1_RX_M0
56	GPIO4_B1/SDMMC1_D1/UART1_TX_M0_u_1.8V	I/O	UP		SDIO0_D1	SDIO0 data port , for WIFI module	1.8V	AP34	GPIO4_B1/SDMMC1_D1/UART1_TX_M0
58	GND_19	G			GND	GND	GND		GND_19
60	RTC_CLKO_WIFI				RTC_CLKO_WIFI	32.768K clock output to WIFI	1.8V		
62	GPIO4_C2/I2C5_SDA_u_1.8V	I/O	UP		BT_REG_ON_H	BT module power enable 1:Enable 0:Disable	1.8V	AL29	GPIO4_C2/I2C5_SDA
64	GPIO4_B4/UART4_RX/SPI1_CLK_M0_u_1.8V	I/O	UP		UART4_RXD	UART0 serial port, for BT module	1.8V	AN33	GPIO4_B4/UART4_RX/SPI1_CLK_M0
66	GPIO4_B5/UART4_TX/SPI1_MOSI_M0_u_1.8V	I/O	UP		UART4_TXD	UART0 serial port, for BT module	1.8V	AJ29	GPIO4_B5/UART4_TX/SPI1_MOSI_M0
68	GPIO4_B6/UART4_CTS/SPI1_CSN0_M0_u_1.8V	I/O	UP		UART4_CTS	UART0 serial port, for BT module	1.8V	AU39	GPIO4_B6/UART4_CTS/SPI1_CSN0_M0
70	GPIO4_B7/UART4_RTS/SPI1_MISO_M0_u_1.8V	I/O	UP		UART4_RTS	UART0 serial port, for BT module	1.8V	AR33	GPIO4_B7/UART4_RTS/SPI1_MISO_M0
72	GPIO4_C3_u_1.8V	I/O	UP		BT_WAKE_L	AP wake up BT module	1.8V	AL27	GPIO4_C3
74	GPIO4_C4_u_1.8V	I/O	UP		BT_HOST_WAKE_L	WIFI module wake up AP	1.8V	AL31	GPIO4_C4
76	GND_20	G			GND	GND	GND		GND_20
78	GPIO2_C6/LCDC_CLK_d_3.3V	I/O	DOWN		3G_PWR_EN	3G power enable	3.3V	AW33	GPIO2_C6/LCDC_CLK
80	GPIO2_C0/CIF_D0/CLKOUT_ETHERNET_d_3.3V	I/O	DOWN		TP_INT1	Touch panel interrupt input (Not debugged)	3.3V	AR25	GPIO2_C0/CIF_D0/CLKOUT_ETHERNET
82	GPIO3_C7/LCDC_D13/UART7_RX/SPI1_CLK_M1_d_3.3V	I/O	DOWN		SPI1_CLK_M1/GPIO3_C7	SPI bus port 2	3.3V	AL35	GPIO3_C7/LCDC_D13/UART7_RX/SPI1_CLK_M1
84	GPIO3_D1/LCDC_D15/PWM9/SPI1_CSN0_M1_d_3.3V	I/O	DOWN		SPI1_CSN0_M1/PWM9	SPI bus port 2	3.3V	AG31	GPIO3_D1/LCDC_D15/PWM9/SPI1_CSN0_M1
86	GPIO3_D2/LCDC_D16/PWM10/SPI1_MISO_M1_d_3.3V	I/O	DOWN		SPI1_MISO_M1/PWM10	SPI bus port 2	3.3V	AK38	GPIO3_D2/LCDC_D16/PWM10/SPI1_MISO_M1
88	GPIO3_D0/LCDC_D14/PWM8/SPI1_MOSI_M1_d_3.3V	I/O	DOWN		SPI1_MOSI_M1/PWM8	SPI bus port 2	3.3V	AJ35	GPIO3_D0/LCDC_D14/PWM8/SPI1_MOSI_M1

Interface definition

90	GPIO0_C7/UART3_RTS_d_3.3V	I/O	DOWN		SDMMC0_PWR	SD card power supply enabled	3.3V	AR13	GPIO0_C7/UART3_RTS
92	NC_58								
94	GPIO0_B7/PWM0/OTG_DRV_d_3.3V	I/O	DOWN		LCD_BL_PWM0	LCD panel backlight brightness control output	3.3V	AV14	GPIO0_B7/PWM0/OTG_DRV
96	GPIO0_C3/PWM1/UART3_TX_d_3.3V	I/O	DOWN		LCD_BL_PWM1	PWM1	3.3V	AV18	GPIO0_C3/PWM1/UART3_TX
98	GPIO1_B0/EMMC_PWREN/SPI2_MOSI_M0_u_3.3V	I/O	UP		GPIO1_B0	GPIO (no used)	3.3V	G31	GPIO1_B0/EMMC_PWREN/SPI2_MOSI_M0
100	GPIO1_B4/SPI0_MOSI/I2C2_SCL_M1/UART1_RX_M1_u_3.3V	I/O	UP		UART1DBG_RX	Uart1 serial port data input, for AP debug	3.3V	C27	GPIO1_B4/SPI0_MOSI/I2C2_SCL_M1/UART1_RX_M1
102	GPIO1_B5/SPI0_MISO/I2C2_SDA_M1/UART1_TX_M1_u_3.3V	I/O	UP		UART1DBG_TX	Uart1 serial port data output ,for AP debug	3.3V	A27	GPIO1_B5/SPI0_MISO/I2C2_SDA_M1/UART1_TX_M1
104	NC_70								
106	GPIO2_C3/CIF_D11/LCDC_D3_d_3.3V	I/O	DOWN		MIPI_PDN0_H	Mipi camera power down，low when the camera is working	3.3V	AL23	GPIO2_C3/CIF_D11/LCDC_D3
108	NC_61								
110	GPIO2_C4/LCDC_D4_d_3.3V	I/O	DOWN		WK2124_INT	INT interrupt trigger, notify CPU, CPU gets related information	3.3V	AL25	GPIO2_C4/LCDC_D4
112	GPIO2_C5/LCDC_D5_d_3.3V	I/O	DOWN		TP_INT	Touch panel interrupt input	3.3V	AW35	GPIO2_C5/LCDC_D5
114	NC_62								
116	GPIO3_C4/LCDC_D10/UART6_TX_d_3.3V	I/O	DOWN		WK2124_RST	WK2124 Reset	3.3V	AL39	GPIO3_C4/LCDC_D10/UART6_TX
118	GPIO3_C5/LCDC_D11/UART6_RX_d_3.3V	I/O	DOWN		LCD_RST	LCD Reset	3.3V	AJ33	GPIO3_C5/LCDC_D11/UART6_RX
120	GPIO0_B6/PCIE_PERST_M1_u_3.3V	I/O	UP		PCIE_RST	PCIE Reset	3.3V	AU9	GPIO0_B6/PCIE_PERST_M1
122	NC_63								
124	GND_21	G			GND	GND	GND		GND_21

Interface definition

126	DPHY_TX_D3P	A			MIPI_DSI_D3P	MIPI-DSI0 differential lane 3 positive	1.8V	H38	DPHY_TX_D3P
128	DPHY_TX_D3N	A			MIPI_DSI_D3N	MIPI-DSI0 differential lane 3 negative	1.8V	G39	DPHY_TX_D3N
130	DPHY_TX_D2P	A			MIPI_DSI_D2P	MIPI-DSI0 differential lane 2 positive	1.8V	F38	DPHY_TX_D2P
132	DPHY_TX_D2N	A			MIPI_DSI_D2N	MIPI-DSI0 differential lane 2 negative	1.8V	E39	DPHY_TX_D2N
134	DPHY_TX_CLKP	A			MIPI_DSI_CLKP	MIPI-DSI0 differential clock lane positive	1.8V	G35	DPHY_TX_CLKP
136	DPHY_TX_CLKN	A			MIPI_DSI_CLKN	MIPI-DSI0 differential clock lane negative	1.8V	E35	DPHY_TX_CLKN
138	DPHY_TX_D1P	A			MIPI_DSI_D1P	MIPI-DSI0 differential lane 1 positive	1.8V	D38	DPHY_TX_D1P
140	DPHY_TX_D1N	A			MIPI_DSI_D1N	MIPI-DSI0 differential lane 1 negativ	1.8V	C39	DPHY_TX_D1N
142	DPHY_TX_D0P	A			MIPI_DSI_D0P	MIPI-DSI0 differential lane 0 positive	1.8V	A37	DPHY_TX_D0P
144	DPHY_TX_D0N	A			MIPI_DSI_D0N	MIPI-DSI0 differential lane 0 negativ	1.8V	B38	DPHY_TX_D0N
146	NC_64								
148	NC_65								
150	ADC_IN0	A			ADC_IN0	ADC input , Core board interiorl pull up Resistor 10K	1.8V	W31	ADC_IN0
152	ADC_IN2	A			RECOVER	AD keyboard input， Core board interiorl pull up Resistor 10K	1.8V	W33	ADC_IN2
154	ADC_IN1	A			LINE_IN_DET	LINE_IN detect input， Core board interiorl pull up Resistor 10K	1.8V	U31	ADC_IN1
156	ADC_IN3	A			HP_DET	Headphone insert detect input， Core board interiorl pull up Resistor 10K	1.8V	U33	ADC_IN3
158	GPIO0_C5/PCIE_WAKE_M1/PWM2_d_3.3V	I/O	DOWN		PCIE_WAKE	AP wake up PCIE	3.3V	AV16	GPIO0_C5/PCIE_WAKE_M1/PWM2
160	GPIO0_C6/PCIE_CLKREQN_M1/UART3_CTS_d_3.3V	I/O	DOWN		PCIE_CLKREQ	PCIE CLKREQN	3.3V	AN15	GPIO0_C6/PCIE_CLKREQN_M1/UART3_CTS

Interface definition

162	NC_66								
164	GND_22	G			GND	GND	GND		GND_22
166	GPIO4_A3/SDMMC0_D1/UART2_RX_M0_u_3.3V	I/O	UP		SDMMC0_D1	SDMMC_D1 data port,for TF Card	3.3V	AE35	GPIO4_A3/SDMMC0_D1/UART2_RX_M0
168	GPIO4_A2/SDMMC0_D0/UART2_TX_M0_u_3.3V	I/O	UP		SDMMC0_D0	SDMMC_D0 data port,for TF Card	3.3V	AG39	GPIO4_A2/SDMMC0_D0/UART2_TX_M0
170	GPIO4_A4/SDMMC0_D2/JTAG_TCK_u_3.3V	I/O	UP		SDMMC0_D2	SDMMC_D2 data port,for TF Card	3.3V	AF38	GPIO4_A4/SDMMC0_D2/JTAG_TCK
172	GPIO4_A0/SDMMC0_CMD/TEST_CLK0_u_3.3V	I/O	UP		SDMMC0_CMD	SDMMC command output,for TF Card	3.3V	AJ39	GPIO4_A0/SDMMC0_CMD/TEST_CLK0
174	GPIO4_A5/SDMMC0_D3/JTAG_TMS_u_3.3V	I/O	UP		SDMMC0_D3	SDMMC_D3 data port,for TF Card	3.3V	AE33	GPIO4_A5/SDMMC0_D3/JTAG_TMS
176	GPIO4_A1/SDMMC0_CLK_d_3.3V	I/O	DOWN		SDMMC0_CLK	SDMMC clock output is used for TF card.	3.3V	AH38	GPIO4_A1/SDMMC0_CLK
178	GPIO0_A3/PCIE_CLKREQN_M0/SDMMC0_DETN_u_1.8V	I/O	UP		SDMMC0_DET	Sdmmc card detect signal, 0: TF card insert 1: TF card no insert	1.8V	AV20	GPIO0_A3/PCIE_CLKREQN_M0/SDMMC0_DETN
180	GND_23	G			GND	GND	GND		GND_23
182	GPIO2_B0/CIF_D6/RGMII_MDIO_d_3.3V	I/O	DOWN		MAC_MDIO	MAC management interface data	3.3V	AW29	GPIO2_B0/CIF_D6/RGMII_MDIO
184	GPIO2_B2/CIF_D8/RGMII_MDC/LCDC_HSYNC_M0_d_3.3V	I/O	DOWN		MAC_MDC	MAC management interface clock	3.3V	AW31	GPIO2_B2/CIF_D8/RGMII_MDC/LCDC_HSYNC_M0
186	GPIO2_C1/CIF_D1/RGMII_TXCLK_d_3.3V	I/O	DOWN		PHY_TXCLK	MAC transmit clock	3.3V	AN27	GPIO2_C1/CIF_D1/RGMII_TXCLK
188	GPIO2_C2/CIF_D10/RGMII_RXCLK/LCDC_D2_d_3.3V	I/O	DOWN		MAC_RXCLK	MAC RX clock	3.3V	AN25	GPIO2_C2/CIF_D10/RGMII_RXCLK/LCDC_D2
190	GND_24	G			GND	GND	GND		GND_24
192	GPIO2_B7/CIF_CLKOUT/RGMII_CLK_d_3.3V	I/O	DOWN		MAC_CLK	MAC reference clock output	3.3V	AR27	I/O DOWN
194	GPIO2_A5/CIF_D3/RGMII_RXD1/SPI2_CLK_M1_d_3.3V	I/O	DOWN		MAC_RXD1	MAC receive data	3.3V	AL21	I/O DOWN

Interface definition

196	GPIO2_B6/CIF_CLKIN/RGMII_RXD3_d_3.3V	I/O	DOWN		MAC_RXD3	MAC receive data	3.3V	AU31	I/O DOWN
198	GPIO2_A4/CIF_D2/RGMII_RXD0/SPI2_MISO_M1_d_3.3V	I/O	DOWN		MAC_RXD0	MAC receive data	3.3V	AN21	I/O DOWN
200	GPIO2_B5/CIF_HREF/RGMII_RXD2_d_3.3V	I/O	DOWN		MAC_RXD2	MAC receive data	3.3V	AV32	I/O DOWN
202	GPIO2_A7/CIF_D5/RGMII_RXDV/SPI2_CSN_M1_d_3.3V	I/O	DOWN		MAC_RXDV	MAC receive data valid	3.3V	AU25	I/O DOWN
204	GPIO2_A3/CIF_D15/RGMII_TXD0/LCDC_D1_d_3.3V	I/O	DOWN		PHY_TXD0	MAC transmit data	3.3V	AJ21	I/O DOWN
206	GPIO2_B4/CIF_VSYNC/RGMII_TXD2_d_3.3V	I/O	DOWN		PHY_TXD2	MAC transmit data	3.3V	AV30	I/O DOWN
208	GPIO2_B3/CIF_D9/RGMII_TXD3/LCDC_VSYNC_M0_d_3.3V	I/O	DOWN		PHY_TXD3	MAC transmit data	3.3V	AV28	I/O DOWN
210	GPIO2_A2/CIF_D14/RGMII_TXD1/LCDC_D0_d_3.3V	I/O	DOWN		PHY_TXD1	MAC transmit data	3.3V	AL19	I/O DOWN
212	GPIO2_A1/CIF_D13/RGMII_TXEN/LCDC_D7_d_3.3V	I/O	DOWN		PHY_TXEN	MAC transmit enable	3.3V	AR19	I/O DOWN
214	GPIO2_A6/CIF_D4/RGMII_RXER/SPI2_MOSI_M1_d_3.3V	I/O	DOWN		FAN_CTL	FAN_EN:H	3.3V	AV26	I/O DOWN
216	GPIO2_A0/CIF_D12/RGMII_CRS/LCDC_D6_d_3.3V	I/O	DOWN		PHY_RST	PHY_Reset:L	3.3V	AW25	I/O DOWN
218	NPOR	I	fix up		RESET_KEY	Core board pull up 10K, System reset signal input. 0 : System Reset 1 : Normal	1.8V	AW23	NPOR
220	EXT_EN				PMIC_EXT_EN	External Power enable output,Voltage 5V 1:Enable 0:Disable	5.0V		
222	GND_25	G			GND	GND	GND		GND_25
224	VDDIO_WL_2	P			VDDIO_WL (LDO)	Output Voltage 1.8V,Rated output current 300mA	1.8V		
226	VCC_3V3_S0_2	P			VCC_LAN (LDO)	(VCCIO_3V3) Output Voltage 3.3V,Rated output current 500mA	3.3V		
228	VCCA1V8_CODEC_2	P			VCCA1V8_CODEC (LDO)	Output Voltage 1.8V,Rated output current 300mA	1.8V		

Interface definition

230	VCCA3V0_CODEC_2	P			VCCA3V0_CODEC (LDO)	Output Voltage 3.0V,Rated output current 100mA	3.0V		
232	VCC_RTC	P			VCC_RTC	Input Voltage 3.3V-5.5V, Rated input current 50mA	5.0V		
234	VCC3V3_SYS_2	P			VCC_3V3 (DCDC)	Output Voltage 3.3V,Rated output current 1A	3.3V		
236	SPKP_OUT				SPKP_OUT	Positive speaker driver output.（no used）			
238	SPKN_OUT				SPKN_OUT	Negative speaker driver output.（no used）			
240	HPL_OUT				HPL	Left channel output of the headphone.			
242	HPR_OUT				HPR	Right channel output of the headphone.			
244	GND_26	G			GND	Power ground	GND		GND_26
246	GND_27	G			GND		GND		GND_27
248	GND_28	G			GND		GND		GND_28
250	GND_29	G			GND		GND		GND_29
252	VCC_SYS_6	P			VCC5V0_SYS	System Power supply Input Voltag : Min 4.8V,Typ 5.0V, Max 5.2V Input current: Typ 400mA ;Max 700mA	5.0V		
254	VCC_SYS_7	P			VCC5V0_SYS		5.0V		
256	VCC_SYS_8	P			VCC5V0_SYS		5.0V		
258	VCC_SYS_9	P			VCC5V0_SYS		5.0V		
260	VCC_SYS_10	P			VCC5V0_SYS		5.0V		

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