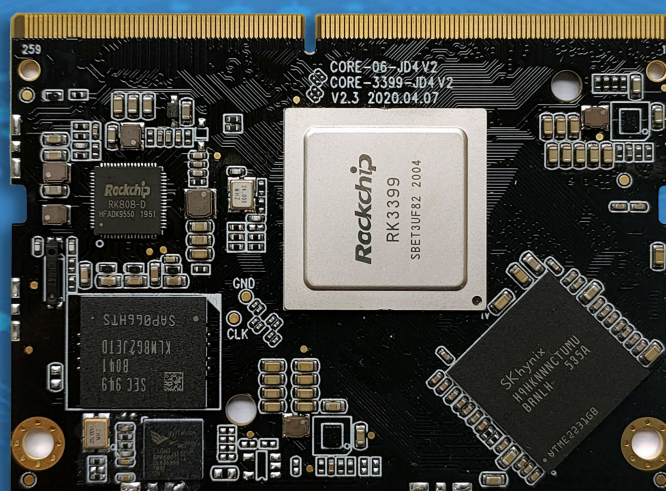


天启科技

Core-3399-JD4V2

六核高性能 AI 核心板

V1.0



天启智能科技有限公司

www.t-firefly.com



更 新 记 录

版 本	更新日期	更新内容
V1.0	2020-5-20	硬件版本为 V2.3



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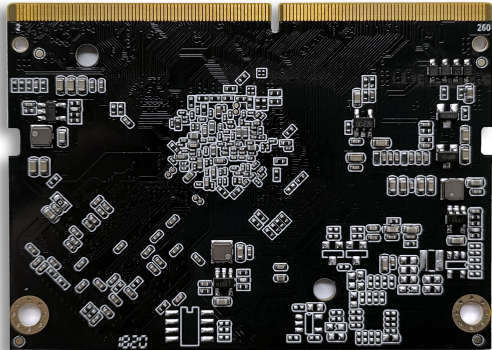
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一、产品简介

采用 Rockchip 高性能六核 64 位处理器 RK3399，支持 AI 神经网络处理器 SPR5801S，高算力、超高效能，强大的硬解码能力、丰富的扩展接口，可应用到集群服务器、计算机视觉、商显一体设备等行业中。



六核 64 位高性能核心板

Core-3399-JD4V2 核心板 采用 RK3399 六核 64 位 (A72×2 + A53×4)处理器，主频高达 1.8GHz，集成四核 Mali-T860 GPU。提供多种存储配置选择，用户仅需扩展功能底板即可快速实现项目研产。

丰富的扩展接口

支持 I2C、SPI、UART、ADC、PWM、GPIO、PCIe、USB3.0、I2S（支持 8 路数字麦克风阵列输入）

强大的硬件编解码能力

支持 4K VP9 and 4K 10bits H265/H264 视频解码，高达 60fps。支持 1080P 多格式视频解码（VC-1, MPEG-1/2/4, VP8）。支持 1080P 视频编码，支持 H.264, VP8 格式。

支持多个操作系统

支持 Android、Linux+QT、Ubuntu 多个操作系统，性能稳定可靠。

搭配高性能行业底板

核心板可与底板组合，构成完整的高性能行业应用主板，扩展接口更丰富，性能更强大，可直接应用到各种智能产品中，加速产品落地。

支持 AI 神经网络加速芯片

支持 AI 神经网络加速芯片 SPR5801S，APiM 架构，算力高达 2.8TOPS，9.3Tops/W 超高效能。支持 PLAI 和 MDK（Caffe）模型训练与转换工具，用于高性能边缘计算领域、基于视觉的深度学习运算和 AI 算法加速。

强大的显示接口

强大的显示接口，支持 MIPI-DSI、EDP、HDMI、DP1.2 多种显示输出接口，支持双屏同显/双屏异显。

沉金接口，稳固可靠、布局紧凑美观

采用 SODIMM 260P 接口，数据传输和扩展性能得到最好发挥，沉金工艺引脚，耐腐蚀，2 螺柱固定，牢固可靠。设计尺寸仅有 69.6mm x 50.27mm，节约更多宝贵的空间。

开放资料

提供配套的源代码、教程、技术资料 and 开发工具，让开发变得更加简单方便。

应用广泛

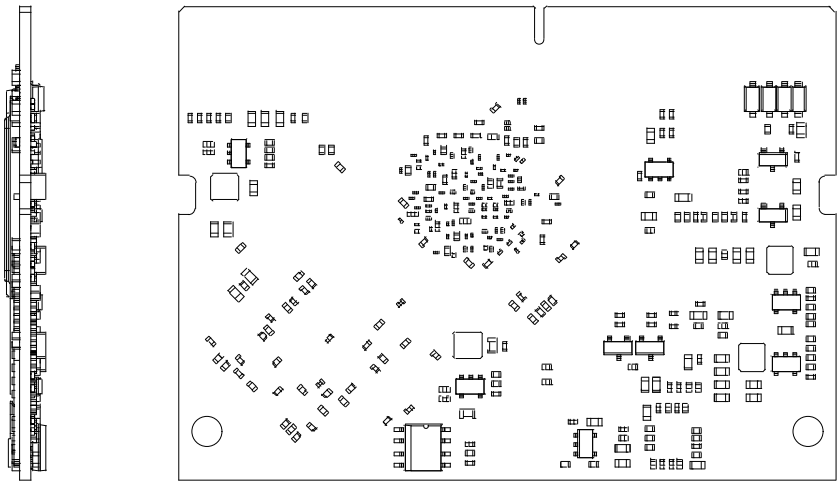
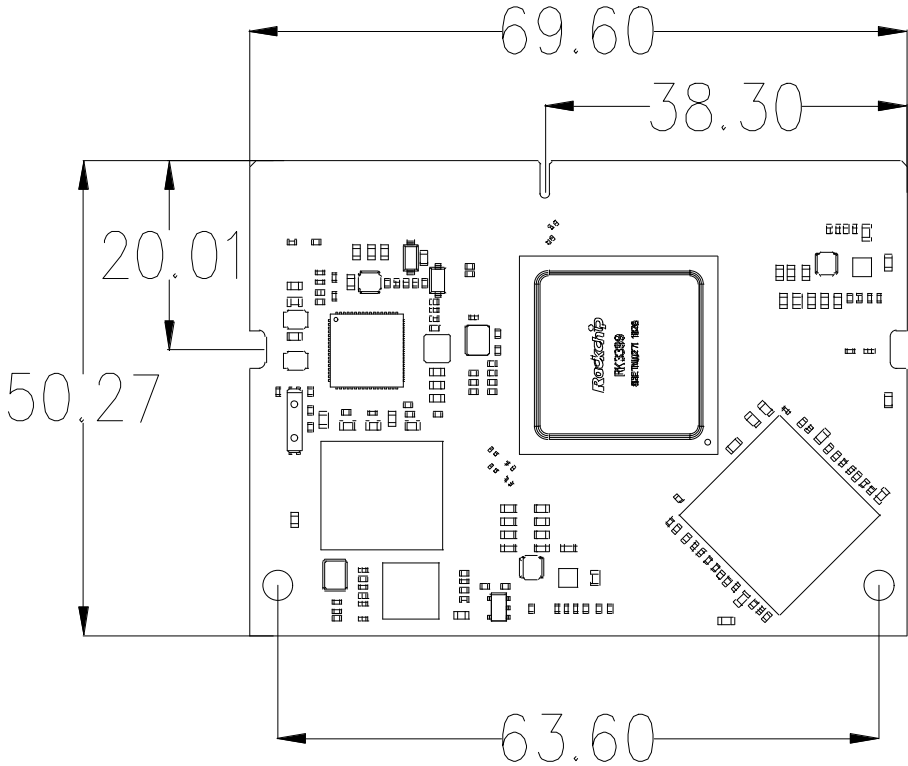
应用到各种行业的产品中集群服务器、高性能计算/存储、计算机视觉、游艺/游戏设备、商显一体设备、医疗健康设备、自动售货机、平板电脑。



二、规格参数

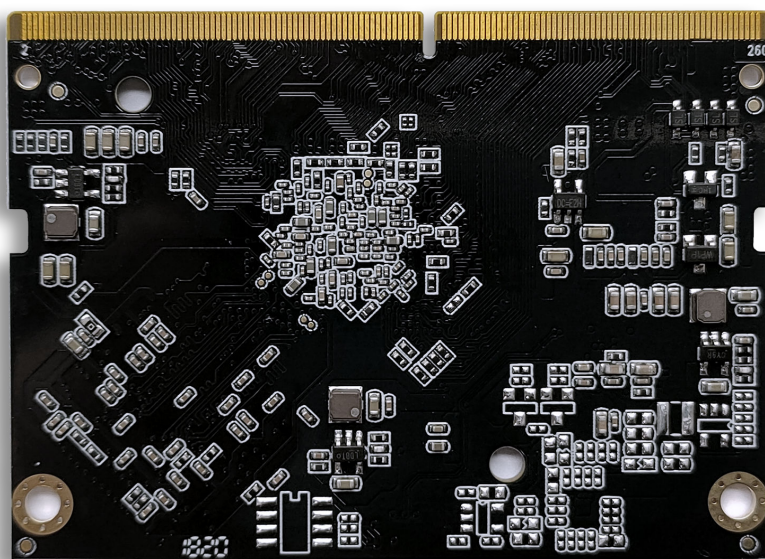
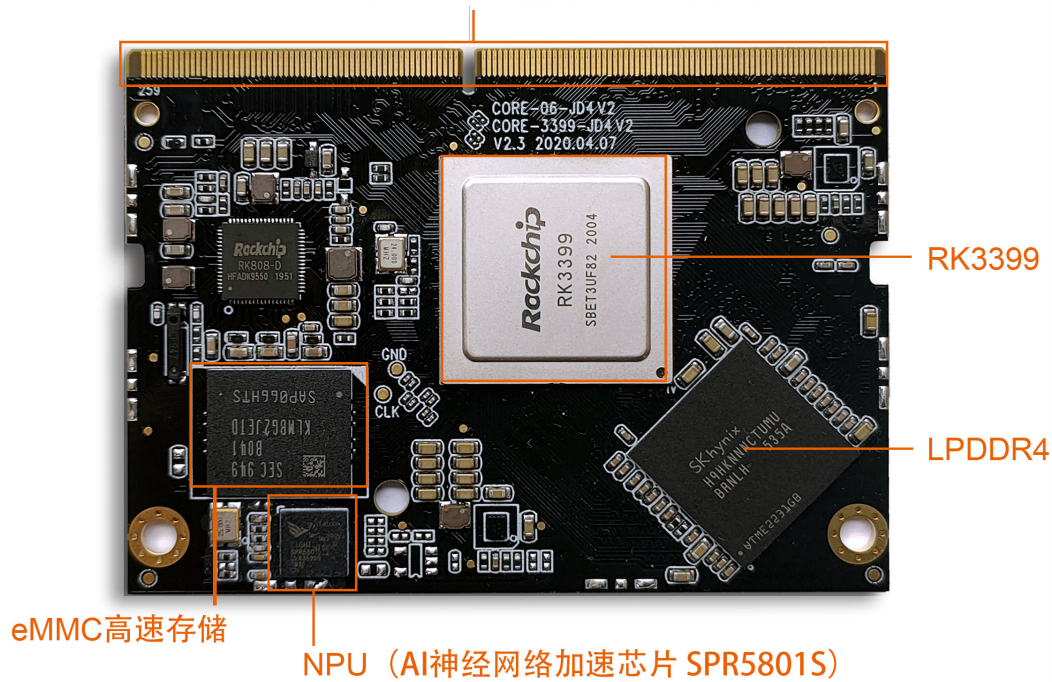
基 本 参 数	
主控芯片	Rockchip RK3399 (28 纳米 HKMG 制程)
处理器	ARM®六核 64 位处理器，主频高达 1.8GHz 基于 big.LITTLE 大小核架构，双核 Cortex-A72(大核)+四核 Cortex-A53(小核)
图形处理器	ARM® Mali-T860 MP4 四核 GPU 支持 OpenGL ES1.1/2.0/3.0/3.1, OpenVG1.1, OpenCL, DX11 支持 AFBC (帧缓冲压缩)
视频处理器	支持 4K VP9 and 4K 10bits H265/H264 视频解码，高达 60fps 1080P 多格式视频解码 (WMV, MPEG-1/2/4, VP8) 1080P 视频编码，支持 H.264, VP8 格式 视频后期处理器：反交错、去噪、边缘/细节/色彩优化
内存	4GB LPDDR4 (2GB/4GB 可选配)
存储器	32GB 高速 eMMC 5.1 (16GB/32GB/128GB 可选配) 支持 TF 卡扩展、支持 M.2 PCIe M-KEY 扩展 NVMe 协议 SSD
NPU	SPR5801S 神经网络 AI 加速芯片 (可选配) ● 峰值算力高达 2.8 Tops, 9.3Tops/W 的超高效能 ● 支持 PLAI (PyTorch)、MDK (Caffe)模型训练与转换工具、TensorFlow ● 现支持图片分类模型：VGG-16(GNet1)、GNet18 和 GNetfc，目标检测模型：SSD(基于 VGG)
硬 件 特 性	
以太网	集成 GMAC 以太网控制器 支持扩展 RTL8211F 实现 10/100/1000Mbps 以太网
WiFi	通过 SDIO3.0 扩展 WiFi & Bluetooth
显示	1 x HDMI 2.0，支持 4K@60HZ 输出 和 HDCP 1.4/2.2 1 x MIPI-DSI，支持单通道 2560x1600@60fps 输出 1 x eDP 1.3 (4 lanes with 10.8Gbps) 1 x DP 1.2 (DisplayPort)，支持 4K@60 fps 输出 支持双屏同显、双屏异显
音频	1 x HDMI 2.0 音频输出 1 x SPDIF 数字音频接口，用于音频输出 2 x I2S 用于音频输入输出
摄像头	2x MIPI-CSI 摄像头接口 (内置双硬件 ISP，最高支持单 13Mpixel 或 双 8Mpixel)
USB	3 x USB2.0 (若选配 NPU，会占用 1 个 USB2.0) 1 x USB3.0
其它接口	I2C×8、SPI×5、UART×5、ADC×4、PWM×3、GPIO×107、PCIe×1、I2S×2 (支持 8 路数字麦克风阵列输入)
电源	DC 输入电压 5V
系 统 软 件	
系统支持	Android 、Linux+QT、Ubuntu
外 观 规 格	
核心板尺寸	69.60 mm × 50.27 mm
接口类型	金手指 (SODIMM 260P 标准接口， 0.5mm 间距)
PCB 规格	8 层板设计

三、规格尺寸

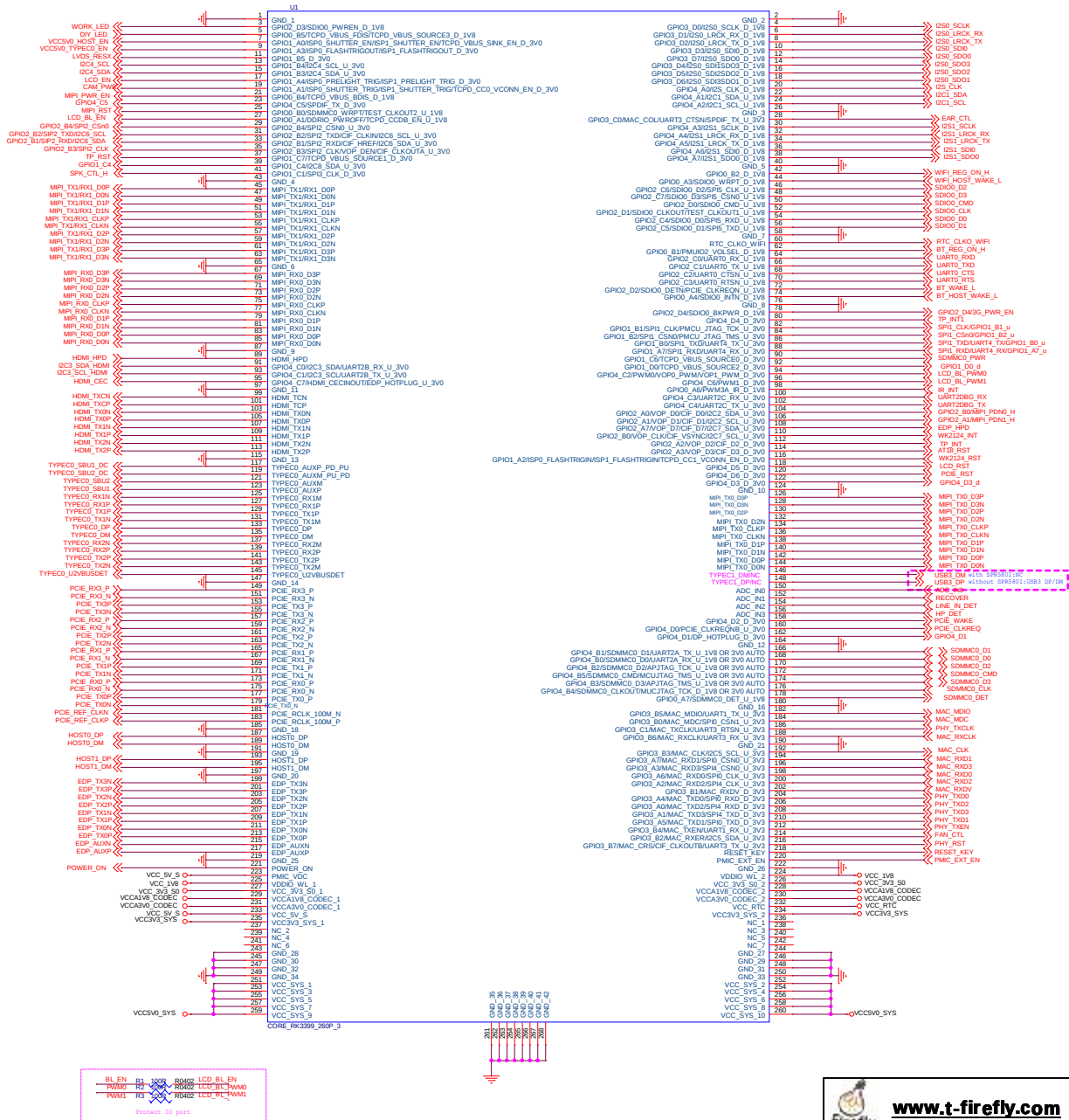


四、接口描述

SODIMM接口定义 (标准260Pin接口)



五、接口定义




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Title: MXM Connector	
File: MB-J04-RK33983398PRO	Rev: ver
Create Date: Tuesday, October 10, 2018	Page: Num 10
dw	13 2020
dw	1: 28

接口定义

Notes1: Pin type: I = input, O = output, I/O = input/output (bidirectional) ,G= Ground , P = power supply , DOWN = Internal pull down , UP = Internal pull UP								
pin	Core board pin definition	Pin type	I/O Pull	Function for Floor(MB-RK3399-JD4)	Default function description	IO Power domain	RK3399 Pin Number	RK3399 Pin Name
1	GND_1	G		GND	GND			
3	GPIO2_D3/SDIO0_PWREN_D_1.8V	I/O	DOWN	WORK_LED	System LED control 1:Enable 0:Disable	1.8V	AD9	GPIO2_D3/SDIO0_PWREN
5	GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOURCE3_D_1.8V	I/O	DOWN	DIY_LED	Diy led control 1:Enable 0:Disable	1.8V	P24	GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOURCE3
7	GPIO1_A0/ISP0_SHUTTER_EN/ISP1_SHUTTER_EN/TCPD_VBUS_SINK_EN_D_3.0V	I/O	DOWN	VCC5V0_HOST_EN	Host usb 5v power enable 1:Enable 0:Disable Core board internal series resistance 33R	3.0V	R25	GPIO1_A0/ISP0_SHUTTER_EN/ISP1_SHUTTER_EN/TCPD_VBUS_SINK_EN
9	GPIO1_A3/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT_D_3.0V	I/O	DOWN	VCC5V0_TYPEC0_EN	OTG 5v power enable 1:Enable 0:Disable Core board internal series resistance 33R	3.0V	R27	GPIO1_A3/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT
11	GPIO1_B5_D_3.0V	I/O	DOWN	LVDS_RESX	LVDS Reset	3.0V	M24	GPIO1_B5
13	GPIO1_B4/I2C4_SCL_U_3.0V	I/O	UP	I2C4_SCL	I2C clock , Core board interiorl pull up Resistor 2.2K	3.0V	P30	GPIO1_B4/I2C4_SCL
15	GPIO1_B3/I2C4_SDA_U_3.0V	I/O	UP	I2C4_SDA	I2C data , Core board interiorl pull up Resistor 2.2K	3.0V	P31	GPIO1_B3/I2C4_SDA
17	GPIO1_A4/ISP0_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG_D_3.0V	I/O	DOWN	LCD_EN	LCD enable , Core board internal series resistance 33R	3.0V	R28	GPIO1_A4/ISP0_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG
19	GPIO1_A1/ISP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CC0_VCONN_EN_D_3.0V	I/O	DOWN	CAM_PWR	Camera power enable , Core board internal series resistance 33R	3.0V	T31	GPIO1_A1/ISP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CC0_VCONN_EN
21	GPIO0_B4/TCPD_VBUS_BDIS_D_1.8V	I/O	DOWN	MIPI_PWR_EN	MIPI power enable	1.8V	V26	GPIO0_B4/TCPD_VBUS_BDIS
23	GPIO4_C5/SPDIF_TX_D_3.0V	I/O	DOWN	GPIO4_C5	GPIO	3.0V	AK1	GPIO4_C5/SPDIF_TX
25	GPIO0_B0/SDMMC0_WRPT/TEST_CLKOUT2_U_1.8V	I/O	UP	MIPI_RST	Mipi reset	1.8V	U28	GPIO0_B0/SDMMC0_WRPT/TEST_CLKOUT2
27	GPIO0_A1/DDRIO_PWROFF/TCPD_CCDB_EN_U_1.8V	I/O	UP	LCD_BL_EN	LCD panel power enable	1.8V	R29	GPIO0_A1/DDRIO_PWROFF/TCPD_CCDB_EN
29	GPIO2_B4/SPI2_CSN0_U_3.0V	I/O	UP	GPIO2_B4/SPI2_CSn0	SPI bus port 2	3.0V	F31	GPIO2_B4/SPI2_CSN0
31	GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL_U_3.0V	I/O	UP	GPIO2_B2/SIP2_TXD/I2C6_SCL	SPI bus port 2, I2C serial port 6,need external pull-up	3.0V	H24	GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL
33	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA_U_3.0V	I/O	UP	GPIO2_B1/SIP2_RXD/I2C6_SDA	SPI bus port 2, I2C serial port 6,need external pull-up	3.0V	F30	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA

35	GPIO2_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUTA_U_3.0V	I/O	UP	GPIO2_B3/SPI2_CLK	GPIO / SP2 CLK / MIPI CLK	3.0V	H31	GPIO2_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUTA
37	GPIO1_C7/TCPD_VBUS_SOURCE1_D_3.0V	I/O	DOWN	TP_RST	TP Reset(Active Low)	3.0V	M31	GPIO1_C7/TCPD_VBUS_SOURCE1
39	GPIO1_C4/I2C8_SDA_U_3.0V	I/O	UP	GPIO1_C4	GPIO	3.0V	M29	GPIO1_C4/I2C8_SDA
41	GPIO1_C1/SPI3_CLK_D_3.0V	I/O	DOWN	GPIO1_C1	GPIO	3.0V	M27	GPIO1_C1/SPI3_CLK
43	GND_4	G		GND	GND			
45	MIPI_TX1/RX1_D0P	I/O		MIPI_TX1/RX1_D0P	MIPI-DSI1/CSI1 differential lane 0 positive	1.8V	AK6	MIPI_TX1/RX1_D0P
47	MIPI_TX1/RX1_D0N	I/O		MIPI_TX1/RX1_D0N	MIPI-DSI1/CSI1 differential lane 0 negative	1.8V	AL6	MIPI_TX1/RX1_D0N
49	MIPI_TX1/RX1_D1P	I/O		MIPI_TX1/RX1_D1P	MIPI-DSI1/CSI1 differential lane 1 positive	1.8V	AK7	MIPI_TX1/RX1_D1P
51	MIPI_TX1/RX1_D1N	I/O		MIPI_TX1/RX1_D1N	MIPI-DSI1/CSI1 differential lane 1 negative	1.8V	AL7	MIPI_TX1/RX1_D1N
53	MIPI_TX1/RX1_CLKP	I/O		MIPI_TX1/RX1_CLKP	MIPI-DSI1/CSI1 differential clock lane positive	1.8V	AK8	MIPI_TX1/RX1_CLKP
55	MIPI_TX1/RX1_CLKN	I/O		MIPI_TX1/RX1_CLKN	MIPI-DSI1/CSI1 differential clock lane negative	1.8V	AL8	MIPI_TX1/RX1_CLKN
57	MIPI_TX1/RX1_D2P	I/O		MIPI_TX1/RX1_D2P	MIPI-DSI1/CSI1 differential lane 2 positive	1.8V	AK9	MIPI_TX1/RX1_D2P
59	MIPI_TX1/RX1_D2N	I/O		MIPI_TX1/RX1_D2N	MIPI-DSI1/CSI1 differential lane 2 negative	1.8V	AL9	MIPI_TX1/RX1_D2N
61	MIPI_TX1/RX1_D3P	I/O		MIPI_TX1/RX1_D3P	MIPI-DSI1/CSI1 differential lane 3 positive	1.8V	AK10	MIPI_TX1/RX1_D3P
63	MIPI_TX1/RX1_D3N	I/O		MIPI_TX1/RX1_D3N	MIPI-DSI1/CSI1 differential lane 3 negative	1.8V	AL10	MIPI_TX1/RX1_D3N
65	GND_6	G		GND	GND			
67	MIPI_RX0_D3P	I		MIPI_RX0_D3P	MIPI-CSIO differential lane 3 positive	1.8V	AK11	MIPI_RX0_D3P
69	MIPI_RX0_D3N	I		MIPI_RX0_D3N	MIPI-CSIO differential lane 3 positive	1.8V	AL11	MIPI_RX0_D3N
71	MIPI_RX0_D2P	I		MIPI_RX0_D2P	MIPI-CSIO differential lane 2 positive	1.8V	AK12	MIPI_RX0_D2P
73	MIPI_RX0_D2N	I		MIPI_RX0_D2N	MIPI-CSIO differential lane 2 negative	1.8V	AL12	MIPI_RX0_D2N
75	MIPI_RX0_CLKP	I		MIPI_RX0_CLKP	MIPI-CSIO differential clock lane positive	1.8V	AK13	MIPI_RX0_CLKP
77	MIPI_RX0_CLKN	I		MIPI_RX0_CLKN	MIPI-CSIO differential clock lane negative	1.8V	AL13	MIPI_RX0_CLKN
79	MIPI_RX0_D1P	I		MIPI_RX0_D1P	MIPI-CSIO differential lane 1 positive	1.8V	AK14	MIPI_RX0_D1P
81	MIPI_RX0_D1N	I		MIPI_RX0_D1N	MIPI-CSIO differential lane 1 negative	1.8V	AL14	MIPI_RX0_D1N
83	MIPI_RX0_D0P	I		MIPI_RX0_D0P	MIPI-CSIO differential lane 0 positive	1.8V	AK15	MIPI_RX0_D0P
85	MIPI_RX0_D0N	I		MIPI_RX0_D0N	MIPI-CSIO differential lane 0 negative	1.8V	AL15	MIPI_RX0_D0N
87	GND_9	G		GND	GND			
89	HDMI_HPD	I		HDMI_HPD	HDMI Hot Plug Detection interrupt with 5V tolerance	HDMI_DE T_IN	AE15	HDMI_HPD
91	GPIO4_C0/I2C3_SDA/UART2B_RX_U_3.0V	I/O	UP	I2C3_SDA_HDMI	I2C serial port 3,for HDMI, need external pull-up	3.0V	AG6	GPIO4_C0/I2C3_SDA/UART2B_RX

93	GPIO4_C1/I2C3_SCL/UART2B_TX_U_3.0V	I/O	UP	I2C3_SCL_HDMI	I2C serial port 3,for HDMI, need external pull-up	3.0V	AL2	GPIO4_C1/I2C3_SCL/UART2B_TX
95	GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG_U_3.0V	I/O	UP	HDMI_CEC	HDMI CEC communication	3.0V	AD7	GPIO4_C7/HDMI_CECINOUT/EDP_HOT PLUG
97	GND_11	G		GND	GND			
99	HDMI_TCN	O		HDMI_TXCN	HDMI differential pixel clock negative	1.8V	AL16	HDMI_TCN
101	HDMI_TCP	O		HDMI_TXCP	HDMI differential pixel clock positive	1.8V	AK16	HDMI_TCP
103	HDMI_TX0N	O		HDMI_TX0N	HDMI channel 0 differential serial data negative	1.8V	AL17	HDMI_TX0N
105	HDMI_TX0P	O		HDMI_TX0P	HDMI channel 0 differential serial data positive	1.8V	AK17	HDMI_TX0P
107	HDMI_TX1N	O		HDMI_TX1N	HDMI channel 1 differential serial data negative	1.8V	AL18	HDMI_TX1N
109	HDMI_TX1P	O		HDMI_TX1P	HDMI channel 1 differential serial data positive	1.8V	AK18	HDMI_TX1P
111	HDMI_TX2N	O		HDMI_TX2N	HDMI channel 2 differential serial data negative	1.8V	AL19	HDMI_TX2N
113	HDMI_TX2P	O		HDMI_TX2P	HDMI channel 2 differential serial data positive	1.8V	AK19	HDMI_TX2P
115	GND_13	G		GND	GND			
117	TYPEC0_AUXP_PD_PU			TYPEC0_SBU1_DC	TYPEC0 AUX pull-up/pull-down polarity reversal pins.		AH17	TYPEC0_AUXP_PD_PU
119	TYPEC0_AUXM_PU_PD			TYPEC0_SBU2_DC	TYPEC0 AUX pull-up/pull-down polarity reversal pins.		AG17	TYPEC0_AUXM_PU_PD
121	TYPEC0_AUXM	I/O		TYPEC0_SBU2	TYPEC0 AUX differential TX/RX serial data		AL20	TYPEC0_AUXM
123	TYPEC0_AUXP	I/O		TYPEC0_SBU1	TYPEC0 AUX differential TX/RX serial data		AK20	TYPEC0_AUXP
125	TYPEC0_RX1M	I		TYPEC0_RX1N	TYPEC0 negative half of first Super Speed RX differential pair		AL21	TYPEC0_RX1M
127	TYPEC0_RX1P	I		TYPEC0_RX1P	TYPEC0 positive half of first Super Speed RX differential pair		AK21	TYPEC0_RX1P
129	TYPEC0_TX1P	O		TYPEC0_TX1P	TYPEC0 positive half of first Super Speed TX differential pair.		AL22	TYPEC0_TX1P
131	TYPEC0_TX1M	O		TYPEC0_TX1N	TYPEC0 negative half of first Super Speed TX differential pair		AK22	TYPEC0_TX1M
133	TYPEC0_DP	A		TYPEC0_DP	TYPEC0 Data Plus port(for system update)		AG23	TYPEC0_DP
135	TYPEC0_DM	A		TYPEC0_DM	TYPEC0 Data Minus port(for system update)		AH23	TYPEC0_DN
137	TYPEC0_RX2M	I		TYPEC0_RX2N	TYPEC0 negative half of second SuperSpeedRX differential pair.		AL23	TYPEC0_RX2M
139	TYPEC0_RX2P	I		TYPEC0_RX2P	TYPEC0 positive half of second SuperSpeedRX differential pair.		AK23	TYPEC0_RX2P
141	TYPEC0_TX2P	O		TYPEC0_TX2P	TYPEC0 positive half of second SuperSpeedTX differential pair.		AL24	TYPEC0_TX2P
143	TYPEC0_TX2M	O		TYPEC0_TX2N	TYPEC0 negative half of second SuperSpeedTX differential pair.		AK24	TYPEC0_TX2M

145	TYPEC0_U2VBUSDET	I		TYPEC0_U2VBUSDET	TYPEC0 connected / vbus power detect for USB2.0		AK30	TYPEC0_U2VBUSDET
147	GND_14	G		GND	GND			
149	PCIE_RX3_P	I		PCIE_RX3_P	PCIE differential lane 3 positive input	1.8V	AF27	PCIE_RX3_P
151	PCIE_RX3_N	I		PCIE_RX3_N	PCIE differential lane 3 negative input	1.8V	AF28	PCIE_RX3_N
153	PCIE_TX3_P	O		PCIE_TX3P	PCIE differential lane 3 positive output	1.8V	AD27	PCIE_TX3_P
155	PCIE_TX3_N	O		PCIE_TX3N	PCIE differential lane 3 negative output	1.8V	AD28	PCIE_TX3_N
157	PCIE_RX2_P	I		PCIE_RX2_P	PCIE differential lane 2 positive input	1.8V	AC27	PCIE_RX2_P
159	PCIE_RX2_N	I		PCIE_RX2_N	PCIE differential lane 2 negative input	1.8V	AC28	PCIE_RX2_N
161	PCIE_TX2_P	O		PCIE_TX2P	PCIE differential lane 2 positive output	1.8V	AA27	PCIE_TX2_P
163	PCIE_TX2_N	O		PCIE_TX2N	PCIE differential lane 2 negative output	1.8V	AA28	PCIE_TX2_N
165	PCIE_RX1_P	I		PCIE_RX1_P	PCIE differential lane 1 positive input	1.8V	AH30	PCIE_RX1_P
167	PCIE_RX1_N	I		PCIE_RX1_N	PCIE differential lane 1 negative input	1.8V	AH31	PCIE_RX1_N
169	PCIE_TX1_P	O		PCIE_TX1P	PCIE differential lane 1 positive output	1.8V	AG30	PCIE_TX1_P
171	PCIE_TX1_N	O		PCIE_TX1N	PCIE differential lane 1 negative output	1.8V	AG31	PCIE_TX1_N
173	PCIE_RX0_P	I		PCIE_RX0_P	PCIE differential lane 0 positive input	1.8V	AF30	PCIE_RX0_P
175	PCIE_RX0_N	I		PCIE_RX0_N	PCIE differential lane 0 negative input	1.8V	AF31	PCIE_RX0_N
177	PCIE_TX0_P	O		PCIE_TX0P	PCIE differential lane 0 positive output	1.8V	AE30	PCIE_TX0_P
179	PCIE_TX0_N	O		PCIE_TX0N	PCIE differential lane 0 negative output	1.8V	AE31	PCIE_TX0_N
181	PCIE_RCLK_100M_N	O		PCIE_REF_CLKN	PCIE 100MHz reference clock as input to PLL	1.8V	AD30	PCIE_RCLK_100M_N
183	PCIE_RCLK_100M_P	O		PCIE_REF_CLKP	PCIE 100MHz reference clock as input to PLL	1.8V	AD31	PCIE_RCLK_100M_P
185	GND_18	G		GND	GND			
187	HOST0_DP			HOST0_DP	USB HOST0 Data Plus port		AB30	USB0_DP
189	HOST0_DM			HOST0_DM	USB HOST0 Data Minus port		AB31	USB0_DN
191	GND_19	G		GND	GND			
193	HOST1_DP			HOST1_DP	USB HOST1 Data Plus port		AA30	USB1_DP
195	HOST1_DM			HOST1_DM	USB HOST1 Data Minus port		AA31	USB1_DN
197	GND_20	G		GND	GND			
199	EDP_TX3N	O		EDP_TX3N	eDP differential lane 3 negative output	1.8V	D31	EDP_TX3N
201	EDP_TX3P	O		EDP_TX3P	eDP differential lane 3 positive output	1.8V	D30	EDP_TX3P
203	EDP_TX2N	O		EDP_TX2N	eDP differential lane 2 negative output	1.8V	C31	EDP_TX2N

205	EDP_TX2P	O		EDP_TX2P	eDP differential lane 2 positive output	1.8V	C30	EDP_TX2P
207	EDP_TX1N	O		EDP_TX1N	eDP differential lane 1 negative output	1.8V	A30	EDP_TX1N
209	EDP_TX1P	O		EDP_TX1P	eDP differential lane 1 positive output	1.8V	B30	EDP_TX1P
211	EDP_TX0N	O		EDP_TX0N	eDP differential lane 0 negative output	1.8V	A29	EDP_TX0N
213	EDP_TX0P	O		EDP_TX0P	eDP differential lane 0 positive output	1.8V	B29	EDP_TX0P
215	EDP_AUXN	I/O		EDP_AUXN	eDP differential AUX channel positive output	1.8V	A28	EDP_AUXN
217	EDP_AUXP	I/O		EDP_AUXP	eDP differential AUX channel negative output	1.8V	B28	EDP_AUXP
219	GND_25	G		GND	GND			
221	POWER_ON			POWER_ON	Power on Signal Input, External connection Power key , active low	POWER_		
223	PMIC_VDC	P		VCC_5V_S	Input Voltage 3.3V-5.5V, Rated input current 50mA	5V		
225	VDDIO_WL_1	P		VDDIO_WL	1.8V output,Max current 1A to WIFI_IO	1.8V		
227	VCC_3V3_S0	P		VCC_LAN	3.3V output,Max current 300mA TO LAN	3.3V		
229	VCCA1V8_CODEC_1	P		VCCA1V8_CODEC	1.8V output,Max current 150mA to Codec	1.8V		
231	VCCA3V0_CODEC_1	P		VCCA3V0_CODEC	3.0V output,Max current 300mA to Codec	3.0V		
233	VCC_5V_S	P		VCC_5V_S	5.0V input, Max current 50mA	5.0V		
235	VCC3V3_SYS_1	P		VCC3V3_SYS	3.3V output,Max current 1A	3.3V		
237	NC_2							
239	NC_4							
241	NC_6							
243	GND_28	G		GND	Power ground			
245	GND_30	G		GND	Power ground			
247	GND_32	G		GND	Power ground			
249	GND_34	G		GND	Power ground			
251	VCC_SYS_1	P		VCC5V0_SYS	Input Voltage 4.8V-5.5V	5.0V		
253	VCC_SYS_3	P		VCC5V0_SYS	Input Voltage 4.8V-5.5V	5.0V		
255	VCC_SYS_5	P		VCC5V0_SYS	Input Voltage 4.8V-5.5V	5.0V		
257	VCC_SYS_7	P		VCC5V0_SYS	Input Voltage 4.8V-5.5V	5.0V		
259	VCC_SYS_9	P		VCC5V0_SYS	Input Voltage 4.8V-5.5V	5.0V		

pin	Core board pin definition	Pad type	IO Pull	Function for Floor(MB-JD4-RK3399&3399PRO)	Default function description	IO Power domain	RK3399 Pin Number	RK3399 Pin Name
2	GND_2	G		GND	GND			
4	GPIO3_D0/I2S0_SCLK_D_1.8V	I/O	DOWN	I2S0_SCLK	I2S 0 serial clock , for audio codec	1.8V	AG3	GPIO3_D0/I2S0_SCLK
6	GPIO3_D1/I2S0_LRCK_RX_D_1.8V	I/O	DOWN	I2S0_LRCK_RX	I2S 0 port , for audio codec	1.8V	AF4	GPIO3_D1/I2S0_LRCK_RX
8	GPIO3_D2/I2S0_LRCK_TX_D_1.8V	I/O	DOWN	I2S0_LRCK_TX	I2S 0 port , for audio codec	1.8V	AJ2	GPIO3_D2/I2S0_LRCK_TX
10	GPIO3_D3/I2S0_SDI0_D_1.8V	I/O	DOWN	I2S0_SDI0	I2S serial data input 0	1.8V	Y7	GPIO3_D3/I2S0_SDI0
12	GPIO3_D7/I2S0_SDO0_D_1.8V	I/O	DOWN	I2S0_SDO0	I2S serial data output 0	1.8V	AH1	GPIO3_D7/I2S0_SDO0
14	GPIO3_D4/I2S0_SDI1SDO3_D_1.8V	I/O	DOWN	I2S0_SDO3	I2S serial data output 3	1.8V	AE5	GPIO3_D4/I2S0_SDI1SDO3
16	GPIO3_D5/I2S0_SDI2SDO2_D_1.8V	I/O	DOWN	I2S0_SDO2	I2S serial data output 2	1.8V	AA6	GPIO3_D5/I2S0_SDI2SDO2
18	GPIO3_D6/I2S0_SDI3SDO1_D_1.8V	I/O	DOWN	I2S0_SDO1	I2S serial data output 1	1.8V	AH2	GPIO3_D6/I2S0_SDI3SDO1
20	GPIO4_A0/I2S_CLK_D_1.8V	I/O	DOWN	I2S_CLK	I2S MCLK, for both I2S0 and I2S1	1.8V	AC7	GPIO4_A0/I2S_CLK
22	GPIO4_A1/I2C1_SDA_U_1.8V	I/O	UP	I2C1_SDA	I2C serial port 1,for Audio, Core board interiorl pull up Resistor 2.2K	1.8V	AG1	GPIO4_A1/I2C1_SDA
24	GPIO4_A2/I2C1_SCL_U_1.8V	I/O	UP	I2C1_SCL	I2C serial port 1,for Audio, Core board interiorl pull up Resistor 2.2K	1.8V	Y6	GPIO4_A2/I2C1_SCL
26	GND_3	G		GND	GND			
28	GPIO3_C0/MAC_COL/UART3_CTSN/SPDIF_TX_U_3.3V	I/O	UP	EAR_CTL	EARPHONE out EN (Active high)	3.3V	D27	GPIO3_C0/MAC_COL/UART3_CTSN/SPDIF_TX
30	GPIO4_A3/I2S1_SCLK_D_1.8V	I/O	DOWN	I2S1_SCLK	I2S 1 port,	1.8V	AF3	GPIO4_A3/I2S1_SCLK
32	GPIO4_A4/I2S1_LRCK_RX_D_1.8V	I/O	DOWN	I2S1_LRCK_RX	I2S 1 port,	1.8V	AA7	GPIO4_A4/I2S1_LRCK_RX
34	GPIO4_A5/I2S1_LRCK_TX_D_1.8V	I/O	DOWN	I2S1_LRCK_TX	I2S 1 port,	1.8V	AJ1	GPIO4_A5/I2S1_LRCK_TX
36	GPIO4_A6/I2S1_SDI0_D_1.8V	I/O	DOWN	I2S1_SDI0	I2S 1 port,	1.8V	AD6	GPIO4_A6/I2S1_SDI0
38	GPIO4_A7/I2S1_SDO0_D_1.8V	I/O	DOWN	I2S1_SDO0	I2S 1 port,	1.8V	AC6	GPIO4_A7/I2S1_SDO0
40	GND_5	G		GND	GND			
42	GPIO0_B2_D_1.8V	I/O	DOWN	WIFI_REG_ON_H	WIFI module power enable(active high)	1.8V	W31	GPIO0_B2
44	GPIO0_A3/SDIO0_WRPT_D_1.8V	I/O	DOWN	WIFI_HOST_WAKE_L	WIFI module wake up AP(Wifi-->RK3399)	1.8V	V31	GPIO0_A3/SDIO0_WRPT
46	GPIO2_C6/SDIO0_D2/SPI5_CLK_U_1.8V	I/O	UP	SDIO0_D2	SDIO0 data2 , for WIFI module	1.8V	AG7	GPIO2_C6/SDIO0_D2/SPI5_CLK
48	GPIO2_C7/SDIO0_D3/SPI5_CSN0_U_1.8V	I/O	UP	SDIO0_D3	SDIO0 data3 , for WIFI module	1.8V	AE8	GPIO2_C7/SDIO0_D3/SPI5_CSN0
50	GPIO2_D0/SDIO0_CMD_U_1.8V	I/O	UP	SDIO0_CMD	SDIO0 command output , for WIFI module	1.8V	AH6	GPIO2_D0/SDIO0_CMD
52	GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1_U_1.8V	I/O	UP	SDIO0_CLK	SDIO0 clock output, for WIFI module	1.8V	AF7	GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1

54	GPIO2_C4/SDIO0_D0/SPI5_RXD_U_1.8V	I/O	UP	SDIO0_D0	SDIO0 data0 , for WIFI module	1.8V	AD8	GPIO2_C4/SDIO0_D0/SPI5_RXD
56	GPIO2_C5/SDIO0_D1/SPI5_TXD_U_1.8V	I/O	UP	SDIO0_D1	SDIO0 data1, for WIFI module	1.8V	AK5	
58	GND_7	G		GND	GND			
60	RTC_CLKO_WIFI			RTC_CLKO_WIFI	32.768K clock output to WIFI Core board interiorl pull up Resistor 10K	1.8V		
62	GPIO0_B1/PMUIO2_VOLSEL_D_1.8V	I/O	DOWN	BT_REG_ON_H	BT module power enable 1:Enable 0:Disable Core board interiorl pull up Resistor 10K	1.8V	V30	GPIO0_B1/PMUIO2_VOLSEL
64	GPIO2_C0/UART0_RX_U_1.8V	I/O	UP	UART0_RXD	UART0 RX, for BT module	1.8V	AE9	GPIO2_C0/UART0_RX
66	GPIO2_C1/UART0_TX_U_1.8V	I/O	UP	UART0_TXD	UART0 RX, for BT module	1.8V	AH8	GPIO2_C1/UART0_TX
68	GPIO2_C2/UART0_CTSN_U_1.8V	I/O	UP	UART0_CTS	UART0 CTS, for BT module(hardware flow control)	1.8V	AG8	GPIO2_C2/UART0_CTSN
70	GPIO2_C3/UART0_RTSN_U_1.8V	I/O	UP	UART0_RTS	UART0 RTS, for BT module(hardware flow control)	1.8V	AL5	GPIO2_C3/UART0_RTSN
72	GPIO2_D2/SDIO0_DETN/PCIE_CLKREQN_U_1.8V	I/O	UP	BT_WAKE_L	AP wake up BT module	1.8V	AL4	GPIO2_D2/SDIO0_DETN/PCIE_CLKREQN
74	GPIO0_A4/SDIO0_INTN_D_1.8V	I/O	DOWN	BT_HOST_WAKE_L	BT module wake up AP	1.8V	AA25	GPIO0_A4/SDIO0_INTN
76	GND_8	G		GND	GND			
78	GPIO2_D4/SDIO0_BKPWR_D_1.8V	I/O	DOWN	GPIO2_D4/3G_PWR_EN	3G Power_EN (active high)	1.8V	AF8	GPIO2_D4/SDIO0_BKPWR
80	GPIO4_D4_D_3.0V	I/O	DOWN	TP_INT1	Touch pannel interrupt input 1	3.0V	AH5	GPIO4_D4
82	GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK_U_3.0V	I/O	UP	SPI1_CLK/GPIO1_B1_u	SPI bus port 1	3.0V	P28	GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK
84	GPIO1_B2/SPI1_CSN0/PMCU_JTAG_TMS_U_3.0V	I/O	UP	SPI1_CSn0/GPIO1_B2_u	SPI bus port 1	3.0V	P29	GPIO1_B2/SPI1_CSN0/PMCU_JTAG_TMS
86	GPIO1_B0/SPI1_TXD/UART4_TX_U_3.0V	I/O	UP	SPI1_TXD/UART4_TX/GPIO1_B0_u	SPI bus port 1	3.0V	R31	GPIO1_B0/SPI1_TXD/UART4_TX
88	GPIO1_A7/SPI1_RXD/UART4_RX_U_3.0V	I/O	UP	SPI1_RXD/UART4_RX/GPIO1_A7_u	SPI bus port 1	3.0V	P27	GPIO1_A7/SPI1_RXD/UART4_RX
90	GPIO1_C6/TCPD_VBUS_SOURCE0_D_3.0V	I/O	DOWN	SDMMC0_PWR	TF_Card Power_EN (active high)	3.0V	L25	GPIO1_C6/TCPD_VBUS_SOURCE0
92	GPIO1_D0/TCPD_VBUS_SOURCE2_D_3.0V	I/O	DOWN	GPIO1_D0_d	GPIO	3.0V	L26	GPIO1_D0/TCPD_VBUS_SOURCE2
94	GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM_D_3.0V	I/O	DOWN	LCD_BL_PWM0	PWM0 output:EDP backlight control(external)	3.0V	AF5	GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM
96	GPIO4_C6/PWM1_D_3.0V	I/O	DOWN	LCD_BL_PWM1	PWM1 output:MIPI backlight control	3.0V	AL3	GPIO4_C6/PWM1
98	GPIO0_A6/PWM3A_IR_D_1.8V	I/O	DOWN	IR_INT	IR receiver input	1.8V	P25	GPIO0_A6/PWM3A_IR
100	GPIO4_C3/UART2C_RX_U_3.0V	I/O	UP	UART2DBG_RX	Uart2 serial port data input, for AP debug	3.0V	AK2	GPIO4_C3/UART2C_RX
102	GPIO4_C4/UART2C_TX_U_3.0V	I/O	UP	UART2DBG_TX	Uart2 serial port data output ,for AP debug	3.0V	AJ4	GPIO4_C4/UART2C_TX

104	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA_U_3.0V	I/O	UP	GPIO2_B0/MIPI_PDN0_H	MIPI Camera0 enable	3.0V	G31	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA
106	GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL_U_3.0V	I/O	UP	GPIO2_A1/MIPI_PDN1_H	MIPI Camera1 enable	3.0V	H25	GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL
108	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA_U_3.0V	I/O	UP	EDP_HPD	EDP_DET Input	3.0V	G30	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA
110	GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL_U_3.0V	I/O	UP	WK2124_INT	WK2124_INT Input	3.0V	H28	GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL
112	GPIO2_A2/VOP_D2/CIF_D2_D_3.0V	I/O	DOWN	TP_INT	TP_INT Input	3.0V	H30	GPIO2_A2/VOP_D2/CIF_D2
114	GPIO2_A3/VOP_D3/CIF_D3_D_3.0V	I/O	DOWN	AT18_RST	AT18_Reset Output (active low)	3.0V	F28	GPIO2_A3/VOP_D3/CIF_D3
116	GPIO1_A2/ISP0_FLASHTRIGIN/ISP1_FLASHTRIGIN/TCPD_CC1_VCONN_EN_D_3.0V	I/O	DOWN	WK2124_RST	WK2124_Reset Output (active low)	3.0V	R26	GPIO1_A2/ISP0_FLASHTRIGIN/ISP1_FLASHTRIGIN/TCPD_CC1_VCONN_EN
118	GPIO4_D5_D_3.0V	I/O	DOWN	LCD_RST	LCD panel reset output (active low)	3.0V	AJ3	GPIO4_D5
120	GPIO4_D6_D_3.0V	I/O	DOWN	PCIE_RST	PCIE_Reset Output (active low)	3.0V	AG4	GPIO4_D6
122	GPIO4_D3_D_3.0	I/O	DOWN	GPIO4_D3_d	GPIO	3.0V	AK3	GPIO4_D3
124	GND_10	G		GND	GND			
126	MIPI_TX0_D3P	O		MIPI_TX0_D3P	MIPI-DSI0 differential lane 3 positive	1.8V	AG9	MIPI_TX0_D3P
128	MIPI_TX0_D3N	O		MIPI_TX0_D3N	MIPI-DSI0 differential lane 3 negative	1.8V	AH9	MIPI_TX0_D3N
130	MIPI_TX0_D2P	O		MIPI_TX0_D2P	MIPI-DSI0 differential lane 2 positive	1.8V	AG11	MIPI_TX0_D2P
132	MIPI_TX0_D2N	O		MIPI_TX0_D2N	MIPI-DSI0 differential lane 2 negative	1.8V	AH11	MIPI_TX0_D2N
134	MIPI_TX0_CLKP	O		MIPI_TX0_CLKP	MIPI-DSI0 differential clock lane positive	1.8V	AG12	MIPI_TX0_CLKP
136	MIPI_TX0_CLKN	O		MIPI_TX0_CLKN	MIPI-DSI0 differential clock lane negative	1.8V	AH12	MIPI_TX0_CLKN
138	MIPI_TX0_D1P	O		MIPI_TX0_D1P	MIPI-DSI0 differential lane 1 positive	1.8V	AG14	MIPI_TX0_D1P
140	MIPI_TX0_D1N	O		MIPI_TX0_D1N	MIPI-DSI0 differential lane 1 negativ	1.8V	AH14	MIPI_TX0_D1N
142	MIPI_TX0_D0P	O		MIPI_TX0_D0P	MIPI-DSI0 differential lane 0 positive	1.8V	AG15	MIPI_TX0_D0P
144	MIPI_TX0_D0N	O		MIPI_TX0_D0N	MIPI-DSI0 differential lane 0 negativ	1.8V	AH15	MIPI_TX0_D0N
146	TYPEC1_DM/NC			USB3_DM	TYPEC1 Data Minus por		AH24	TYPEC1_DN--without AI NC--with AI
148	TYPEC1_DP/NC			USB3_DP	TYPEC1 Data Plus port		AG24	TYPEC1_DP--without AI NC--with AI
150	ADC_IN0	I		ADC_IN0	ADC0 input,Core board interiorl pull up Resistor 10K	1.8V	AG26	ADC_IN0
152	ADC_IN1	I		RECOVER	ADC0(recover_key) input, Core board interiorl pull up Resistor 10K	1.8V	AH26	ADC_IN1
154	ADC_IN2	I		LINE_IN_DET	ADC2 input, Core board interiorl pull up Resistor 10K	1.8V	AG25	ADC_IN2
156	ADC_IN3	I		HP_DET	AD3C input, Core board interiorl pull up Resistor 10K	1.8V	AG28	ADC_IN3

158	GPIO4_D2_D_3.0V	I/O	DOWN	PCIE_WAKE	AP wake up PCIE Output	3.0V	AH3	GPIO4_D2
160	GPIO4_D0/PCIE_CLKREQNB_U_3.0V	I/O	UP	PCIE_CLKREQ	PCIE CLKREQN Output	3.0V	AE6	GPIO4_D0/PCIE_CLKREQNB
162	GPIO4_D1/DP_HOTPLUG_D_3.0V	I/O	DOWN	GPIO4_D1	GPIO	3.0V	AK4	GPIO4_D1/DP_HOTPLUG
164	GND_12	G		GND	GND			
166	GPIO4_B1/SDMMC0_D1/UART2A_TX_U_3.0V	I/O	UP	SDMMC0_D1	SDMMC0 data1 (TF-Card)	Note 2	Y26	GPIO4_B1/SDMMC0_D1/UART2A_TX
168	GPIO4_B0/SDMMC0_D0/UART2A_RX_U_3.0V	I/O	UP	SDMMC0_D0	SDMMC0 data0 (TF-Card)		Y27	GPIO4_B0/SDMMC0_D0/UART2A_RX
170	GPIO4_B2/SDMMC0_D2/APJTAG_TCK_U_3.0V	I/O	UP	SDMMC0_D2	SDMMC0 data2 (TF-Card)		Y28	GPIO4_B2/SDMMC0_D2/APJTAG_TCK
172	GPIO4_B5/SDMMC0_CMD/MCUJTAG_TMS_U_3.0V	I/O	UP	SDMMC0_CMD	SDMMC0 command output (TF-Card)		V25	GPIO4_B5/SDMMC0_CMD/MCUJTAG_TMS
174	GPIO4_B3/SDMMC0_D3/APJTAG_TMS_U_3.0V	I/O	UP	SDMMC0_D3	SDMMC0 data3 (TF-Card)		U27	GPIO4_B3/SDMMC0_D3/APJTAG_TMS
176	GPIO4_B4/SDMMC0_CLKOUT/MUCJTAG_TCK_D_3.0V	I/O	DOWN	SDMMC0_CLK	SDMMC0 clock output (TF-Card) Core board internal series resistance 22R		V29	GPIO4_B4/SDMMC0_CLKOUT/MUCJTAG_TCK
	Note 2: Default is 3.0V; SDMMC0 1.8V(SDIO3.0 model)/3.0V(SDIO2.0 model) Auto							
178	GPIO0_A7/SDMMC0_DET_U_1.8V	I/O	UP	SDMMC0_DET	SDMMC0 detect input (active low)	1.8V	V28	GPIO0_A7/SDMMC0_DET
180	GND_16	G		GND	GND			
182	GPIO3_B5/MAC_MDIO/UART1_TX_U_3.3V	I/O	UP	MAC_MDIO	MAC management command and data	3.3V	G26	GPIO3_B5/MAC_MDIO/UART1_TX
184	GPIO3_B0/MAC_MDC/SPI0_CSN1_U_3.3V	I/O	UP	MAC_MDC	MAC management clock	3.3V	E29	GPIO3_B0/MAC_MDC/SPI0_CSN1
186	GPIO3_C1/MAC_TXCLK/UART3_RTSN_U_3.3V	I/O	UP	PHY_TXCLK	MAC transmit clock Core board internal series resistance 22R	3.3V	E28	GPIO3_C1/MAC_TXCLK/UART3_RTSN
188	GPIO3_B6/MAC_RXCLK/UART3_RX_U_3.3V	I/O	UP	MAC_RXCLK	MAC receive clock	3.3V	F25	GPIO3_B6/MAC_RXCLK/UART3_RX
190	GND_21	G		GND	GND			
192	GPIO3_B3/MAC_CLK/I2C5_SCL_U_3.3V	I/O	UP	MAC_CLK	MAC reference clock output , I2C serial port 5, need external pull-up Core board internal series resistance 22R	3.3V	G24	GPIO3_B3/MAC_CLK/I2C5_SCL
194	GPIO3_A7/MAC_RXD1/SPI0_CSN0_U_3.3V	I/O	UP	MAC_RXD1	MAC receive data	3.3V	F27	GPIO3_A7/MAC_RXD1/SPI0_CSN0
196	GPIO3_A3/MAC_RXD3/SPI4_CSN0_U_3.3V	I/O	UP	MAC_RXD3	MAC receive data	3.3V	E25	GPIO3_A3/MAC_RXD3/SPI4_CSN0
198	GPIO3_A6/MAC_RXD0/SPI0_CLK_U_3.3V	I/O	UP	MAC_RXD0	MAC receive data	3.3V	E26	GPIO3_A6/MAC_RXD0/SPI0_CLK
200	GPIO3_A2/MAC_RXD2/SPI4_CLK_U_3.3V	I/O	UP	MAC_RXD2	MAC receive data	3.3V	E30	GPIO3_A2/MAC_RXD2/SPI4_CLK
202	GPIO3_B1/MAC_RXDV_D_3.3V	I/O	DOWN	MAC_RXDV	MAC receive data valid	3.3V	C27	GPIO3_B1/MAC_RXDV
204	GPIO3_A4/MAC_TXD0/SPI0_RXD_D_3.3V	I/O	DOWN	PHY_TXD0	MAC transmit data Core board internal series resistance 22R	3.3V	D26	GPIO3_A4/MAC_TXD0/SPI0_RXD
206	GPIO3_A0/MAC_TXD2/SPI4_RXD_D_3.3V	I/O	DOWN	PHY_TXD2	MAC transmit data Core board internal series resistance 22R	3.3V	F24	GPIO3_A0/MAC_TXD2/SPI4_RXD

208	GPIO3_A1/MAC_TXD3/SPI4_TXD_D_3.3V	I/O	DOWN	PHY_TXD3	MAC transmit data Core board internal series resistance 22R	3.3V	H23	GPIO3_A1/MAC_TXD3/SPI4_TXD
210	GPIO3_A5/MAC_TXD1/SPI0_TXD_D_3.3V	I/O	DOWN	PHY_TXD1	MAC transmit data Core board internal series resistance 22R	3.3V	G23	GPIO3_A5/MAC_TXD1/SPI0_TXD
212	GPIO3_B4/MAC_TXEN/UART1_RX_U_3.3V	I/O	UP	PHY_TXEN	MAC transmit enable Core board internal series resistance 22R	3.3V	H22	GPIO3_B4/MAC_TXEN/UART1_RX
214	GPIO3_B2/MAC_RXER/I2C5_SDA_U_3.3V	I/O	UP	FAN_CTL	PHY interrupt input, I2C serial port 5, need external pull-up Core board internal series resistance 22R	3.3V	F23	GPIO3_B2/MAC_RXER/I2C5_SDA
216	GPIO3_B7/MAC_CRCS/CIF_CLKOUTB/UART3_TX_U_3.3V	I/O	UP	PHY_RST	phy reset output(active low)	3.3V	B27	GPIO3_B7/MAC_CRCS/UART3_TX/CIF_CLKOUTB
218	RESET_KEY			RESET_KEY	system reset signal Input, External connection Reset key, active low			
220	PMIC_EXT_EN			PMIC_EXT_EN	External Power enable output, Voltage 5V			
222	GND_26	G		GND	GND			
224	VDDIO_WL_2	P		VDDIO_WL	1.8V output,Max current 1A to WIFI_IO	1.8V_OUT		
226	VCC_3V3_S0_2	P		VCC_LAN	3.3V output,Max current 300mA TO LAN	3.3V_OUT		
228	VCCA1V8_CODEEC_2	P		VCCA1V8_CODEEC	1.8V output,Max current 150mA to Codec	1.8V_OUT		
230	VCCA3V0_CODEEC_2	P		VCCA3V0_CODEEC	3.0V output,Max current 300mA to Codec	3.0V_OUT		
232	VCC_RTC	P		VCC_RTC	5.0V input, Max current 50mA	5.0V_IN		
234	VCC3V3_SYS_2	P		VCC3V3_SYS	3.3V output,Max current 1A	3.3V_OUT		
236	NC_1							
238	NC_3							
240	NC_5							
242	NC_7							
244	GND_27	G		GND	Power ground			
246	GND_29	G		GND	Power ground			
248	GND_31	G		GND	Power ground			
250	GND_33	G		GND	Power ground			
252	VCC_SYS_2	P		VCC5V0_SYS	Input Voltage 4.8V-5.5V	5.0V_IN		
254	VCC_SYS_4	P		VCC5V0_SYS	Input Voltage 4.8V-5.5V	5.0V_IN		
256	VCC_SYS_6	P		VCC5V0_SYS	Input Voltage 4.8V-5.5V	5.0V_IN		
258	VCC_SYS_8	P		VCC5V0_SYS	Input Voltage 4.8V-5.5V	5.0V_IN		
260	VCC_SYS_10	P		VCC5V0_SYS	Input Voltage 4.8V-5.5V	5.0V_IN		

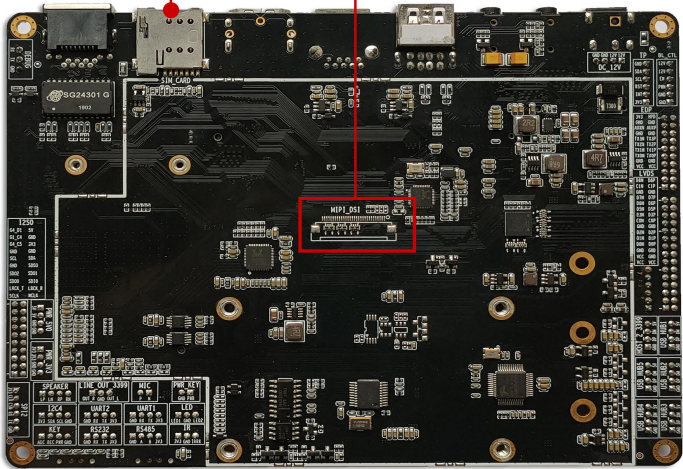


六、核心板与底板

Core-3399-JD4V2核心板与底板组合，构成完整的高性能行业应用主板，
底板同时兼容Core-3399-JD4核心板 和 Core-3399Pro-JD4核心板

PWR_KEY	MIC	Line_Out	Speaker
LED	UART1	UART2	I2C4
IR	RS485	RS232	KEY (ADC/REC/PWR/GND)

SIM卡 (MicroSIM标准) MIPI-DSI



公司简介

天启科技成立于 2009 年，国家高新技术企业，专注于开源智能硬件，人工智能，物联网，数字音频产品的研发设计、生产和销售，同时提供了智能软硬件产品的整体解决方案。开源品牌“Firefly”在互联网上拥有开源社区与网上商城，目前已超过 20 万用户与 5000 多家的企业用户，为众多科技创业者与初创企业加速研发进程，并提供专业的技术服务。

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