

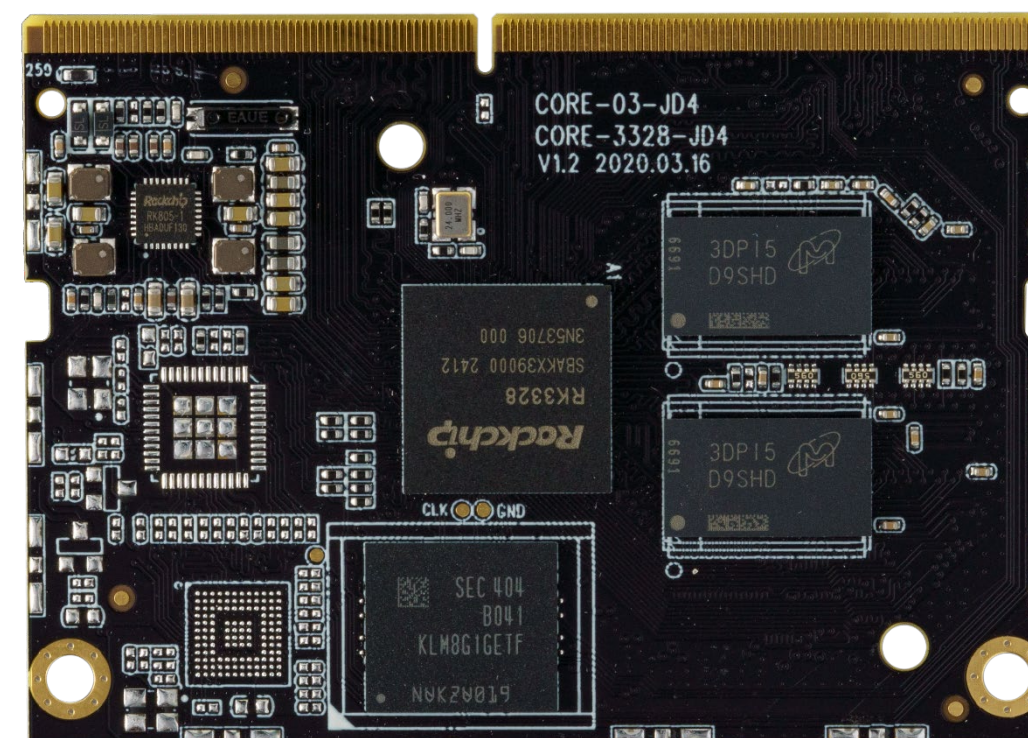


Core-3328-JD4

四核64位入门级核心板

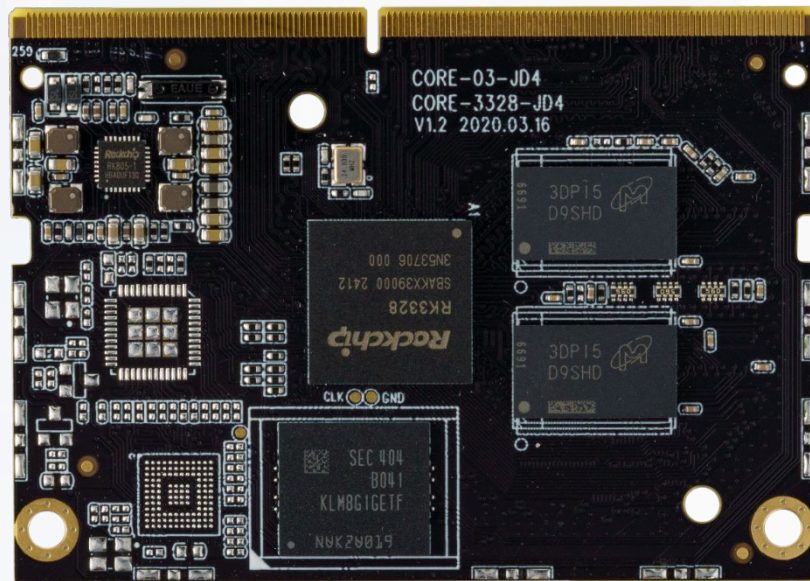
V1.2 2024-10-9

天启智能科技





产品特点 Product features



四核64位处理器

采用四核64位Cortex-A53处理器
RK3328，主频高达1.5GHz，内置双核
Mali-450 GPU



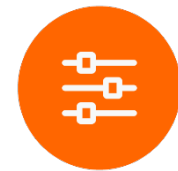
强大的网络通讯能力

支持1路千兆以太网，可通过SDIO3.0信
号扩展WiFi模组，让网络通讯拥有更高
的速率



支持多种操作系统

支持Android、Linux+QT、Ubuntu多
种操作系统，性能稳定可靠，满足不同
场景需求



丰富的扩展接口

拥有HDMI2.0、CVBS、USB3.0、
USB2.0、I2C、SPI、UART、PWM等扩
展接口，满足不同场景的外设扩展需求



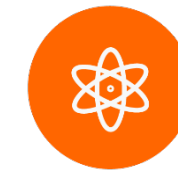
4K H.265 高清视频解码

支持4K@60fps H.265/H.264/VP9视频
解码、1080P@60fps (VC-1, MPEG-
1/2/4)多格式视频解码



沉金接口，稳固可靠

采用 SODIMM 260P 接口，数据传输和
扩展性能得到最好发挥，沉金工艺引脚，
耐腐蚀，2螺柱固定，牢固可靠



高效二次开发自主定制

提供完整技术资料 and 参考设计，用户能
高效进行二次开发，快速打造自主可控
产品



广泛的应用领域

广泛适用于高性能计算/存储、计算机视
觉、游艺/游戏设备、商显一体设备、医
疗健康设备、自动售货机、工业电脑等

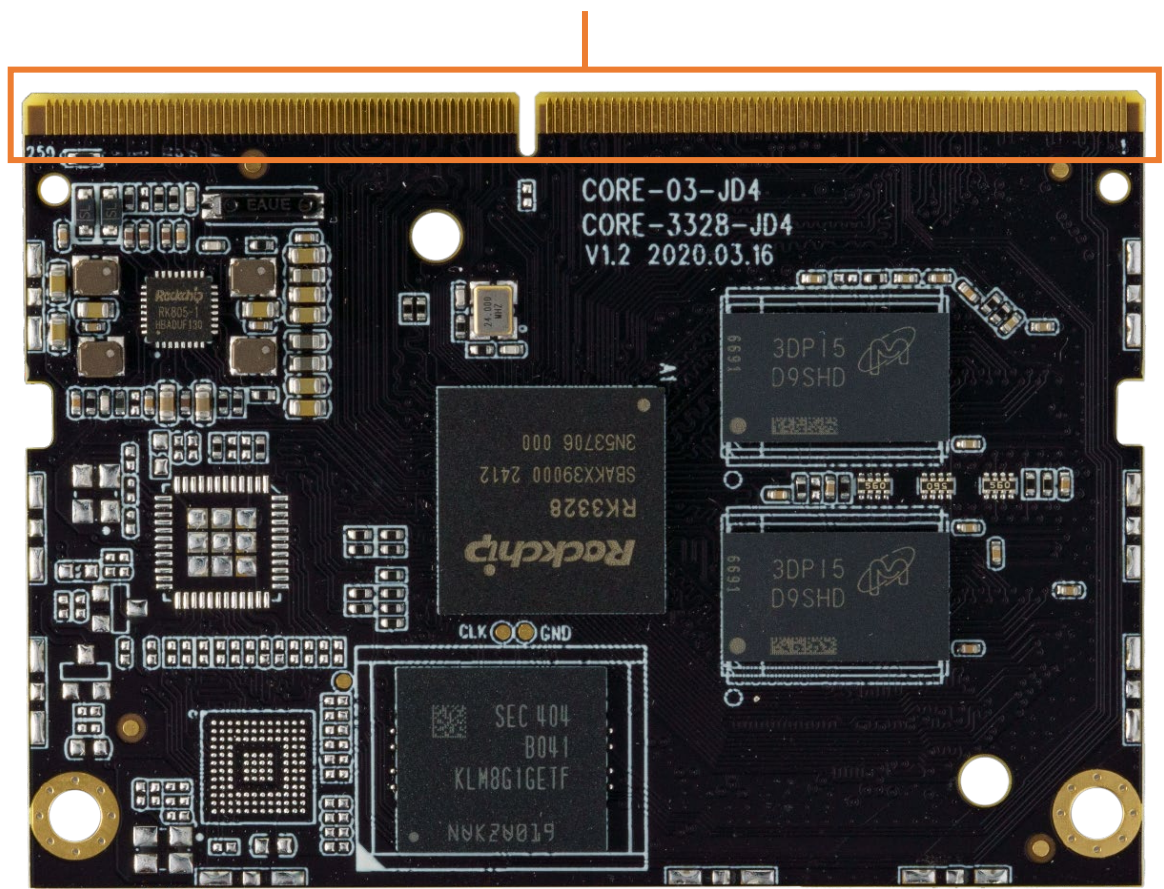
规格参数 Specifications



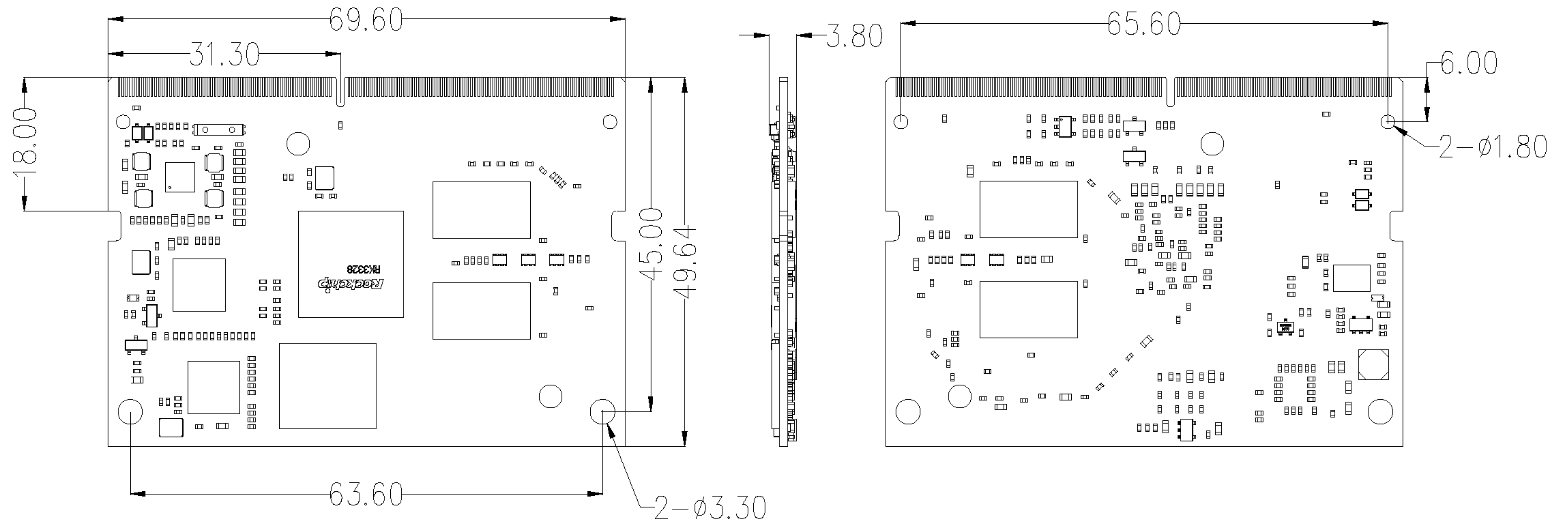
规格参数		
主要参数	SOC	RK3328
	CPU	四核64位ARM® Cortex-A53处理器，主频最高1.5GHz
	GPU	ARM Mali-450 MP2 GPU，支持OpenGL ES1.1/2.0，OpenVG1.1
	编解码	视频解码：4K@60fps H.265/H.264/VP9、1080P@60fps(VC-1, MPEG-1/2/4) 多格式视频解码 视频编码：1080P@30fps H.265/H.264 视频后期处理器：反交错、去噪、边缘/细节/色彩优化
	运行内存	1GB DDR3（1GB/2GB/4GB 可选）
	机身存储	8GB eMMC5.1（8GB/16GB/32GB/64GB/128GB 可选）
	电源	5V（电压误差 ±5%）
	功耗	典型功耗：1.5W(5V/300mA)，最大功耗：3.25W(5V/650mA)
	系统	Android、Ubuntu、Linux+QT
	接口	金手指（SODIMM 260P 标准接口，0.5mm间距）
	尺寸	69.60mm × 49.64mm × 3.80mm
	重量	≈13g
	环境	工作温度：-20℃ ~ 60℃，存储温度：-20℃ ~ 70℃，存储湿度：10% ~ 90%RH（无凝露）
接口参数	以太网	可通过 RGMII 和 RMII 接口扩展1路10/100/1000Mbps以太网
	无线网	通过 SDIO3.0 信号扩展 Wifi 模组
	视频输出	1 × HDMI2.0（4K@60fps） 1 × CVBS（符合480i，576i标准）
	音频	1 × HDMI音频输出 支持 8 通道 I2S/PDM 接口，支持 8 路数字麦克风阵列
	USB	1 × USB3.0 HOST、1 × USB3.0/USB2.0 OTG、2 × USB2.0 HOST
	其他接口	2 × SPI、6 × UART、4 × I2C、8 × PWM、1 × SPDIF、GPIOs

接口描述 Interface description

金手指 (SODIMM 260P 标准接口, 0.5mm间距)



产品尺寸 Dimension





接口定义 Interface definition

Notes1:
Pin type: I = input, O = output, I/O = input/output (bidirectional), G= Ground, P = power supply,
DOWN = Internal pull down , UP = Internal pull UP, 0 = Lowe Level 1 = High level

Part A	pin	Core board pin definition	Pin type	I/O Pull	Default function	Default function description	IO Power domain	RK3328 Pin Number
	1	GND_1	G		GND	GND		
	3	RK805_OUT2			WORK_LED	System working state refers to LED		
	5	RK805_OUT1			DIY_LED	User Defines LED		
	7	USB1_DP			HOST_DP	USB HOST0 Data Plus port (no used)		AA7
	9	USB1_DM			HOST_DM	USB HOST0 Data Minus port (no used)		Y7
	11	NC_1						
	13	GND_2	G		GND	GND		
	15	NC_2						
	17	NC_3						
	19	NC_4						
	21	NC_5						
	23	NC_6						
	25	NC_7						
	27	NC_8						
	29	NC_9						
	31	NC_10						
33	NC_11							



接口定义 Interface definition

	35	GND_3	G		GND	GND		
	37	GPIO1_A5/SDMMC0_DET_N_U_3.3V	I/O	UP	SDMMC0_DET	SDMMC0 card detect signal 0: TF card insert 1: TF card no insert	3.3V	V10
	39	GPIO1_A1/SDMMC0_D1/UART2_RX_M0_U_3.3V	I/O	UP	SDMMC0_D1	SDMMC0 data port	Note 2	W11
	41	GPIO1_A0/SDMMC0_D0/UART2_TX_M0_U_3.3V	I/O	UP	SDMMC0_D0	SDMMC0 data port		U10
	43	GPIO1_A6/SDMMC0_CLK/TEST_CLK0_D_3.3V	I/O	DOWN	SDMMC0_CLK	SDMMC0 clock output		W12
	45	GPIO1_A4/SDMMC0_CMD_U_3.3V	I/O	UP	SDMMC0_CMD	SDMMC0 command output		Y13
	47	GPIO1_A3/SDMMC0_D3/JTAG_TMS_U_3.3V	I/O	UP	SDMMC0_D3/JTAG_TMS	SDMMC0 data port		AA13
	49	GPIO1_A2/SDMMC0_D2/JTAG_TCK_U_3.3V	I/O	UP	SDMMC0_D2/JTAG_TCK	SDMMC0 data port		W13
	Note 2:Default is 3.3V; VCCIO5 Domain 1.8V or 3.3V Power supply, Voltage configure by GPIO0_A7; H = 3.3V, L = 1.8V.							
	51	GND_4	G		GND	GND		
	53	NC_12						
	55	NC_13						
	57	NC_14						
	59	NC_15						
	61	GPIO2_B4/SPI_CSN1_M0/FLASH_VOL_SEL_U_3.3V	I/O	UP	GPIO2_B4/SPI_CSN1_M0/FLASH_VOL_SEL	GPIO (no used)	3.3V	T16
	63	NC_16						
	65	NC_17						
	67	GPIO2_D0/I2C0_SCL/FEPHY_LED_LINK_M1_U_3.3V	I/O	UP	I2C0_SCL	I2C0 data	3.3V	P17
	69	GPIO2_D1/I2C0_SDA/FEPHY_LED_DATA_M1_U_3.3V	I/O	UP	I2C0_SDA	I2C0 clock	3.3V	R17



接口定义 Interface definition

	71	NC_18						
	73	NC_19						
	75	NC_20						
	77	NC_21						
	79	NC_22						
	81	NC_23						
	83	NC_24						
	85	NC_25						
	87	NC_26						
	89	NC_27						
	91	NC_28						
	93	NC_29						
	95	NC_30						
	97	GPIO2_A6/PWM2_U_3.3V	I/O	UP	PWM0/GPIO0_B7	PWM output	3.3V	M19
	99	GPIO0_A0/CLKOUT_WIFI_M0_D_3.3V	I/O	DOWN	VCC5V0_USB30_EN	USB30 5V output power enable 1:Enable 0:Disable	5V	L3
	101	GND_5	G		GND	GND		
	103	NC_31						
	105	NC_32						
	107	NC_33						



接口定义 Interface definition

	109	NC_34						
	111	NC_35						
	113	NC_36						
	115	NC_37						
	117	NC_38						
	119	NC_39						
	121	NC_40						
	123	GND_6	G		GND	GND		
	125	USB30_TXN	I/O		USB30_TXN	USB 3.0 transmission signal DM		H2
	127	USB30_TXP	I/O		USB30_TXP	USB 3.0 transmission signal DP		H3
	129	USB30_RXP	I/O		USB30_RXP	USB 3.0 receive signal DP		J2
	131	USB30_RXN	I/O		USB30_RXN	USB 3.0 receive signal DM		J3
	133	USB0_DP			OTG20_DP	USB 2.0 Data signal DP		AA6
	135	USB0_DM			OTG20_DM	USB 2.0 Data signal DM		Y6
	137	USB30_DP	I/O		USB30_DP	USB 2.0 Data signal DP in USB 3.0 port		K1
	139	USB30_DM	I/O		USB30_DM	USB 2.0 Data signal DM in USB 3.0 port		K2
	141	NC_41						
	143	GND_7	G		GND	GND		
	145	USB20_VBUS	I		OTG_DET	Vbus power detect for USB2.0		T6
	147	GPIO0_A4/HDMI_HPD_D_3.3V	I/O	DOWN	HDMI_HPD	HDMI hot plug detect signal		U3



接口定义 Interface definition

	149	I2C3_SDA/HDMI_SDA_OD_3.3V	I/O		HDMI_SDA	HDMI I2C data line		V3
	151	I2C3_SCL/HDMI_SCL_OD_3.3V	O		HDMI_SCL	HDMI I2C clock		V1
	153	HDMI_CEC_U	I/O	UP	HDMI_CEC	HDMI CEC		V2
	155	GND_8	G		GND	GND		
	157	HDMI_TXCLKN			HDMI_TX_C-	HDMI negative clock line , Core board internal series resistance 0R		W2
	159	HDMI_TXCLKP			HDMI_TX_C+	HDMI positive clock line , Core board internal series resistance 0R		Y1
	161	HDMI_TX0N	O		HDMI_TX_D0-	HDMI channel 0 negative data line		Y2
	163	HDMI_TX0P	O		HDMI_TX_D0+	HDMI channel 0 positive data line		AA2
	165	HDMI_TX1N	O		HDMI_TX_D1-	HDMI channel 1 negative data line		Y3
	167	HDMI_TX1P	O		HDMI_TX_D1+	HDMI channel 1 positive data line		Y4
	169	HDMI_TX2N	O		HDMI_TX_D2-	HDMI channel 2 negative data line		AA4
	171	HDMI_TX2P	O		HDMI_TX_D2+	HDMI channel 2 positive data line		Y5
	173	GND_9	G		GND	GND		
	175	NC_42						
	177	NC_43						
	179	NC_44						
	181	CODEC_AOL	O		AOL	Left channel output of the headphone		P2
	183	CODEC_AOR	O		AOR	Right channel output of the headphone		N1
	185	FEPHY_RXN	I/O		RD-	Receive data - Negative (no used)		AA8
	187	FEPHY_RXP	I/O		RD+	Receive data - Positive (no used)		Y8



接口定义 Interface definition

	189	FEPHY_TXN	I/O		TD-	Transmit data - Negative (no used)		AA9
	191	FEPHY_TXP	I/O		TD+	Transmit data - Positive (no used)		Y9
	193	NC_45						
	195	NC_46						
	197	NC_47						
	199	NC_48						
	201	NC_49						
	203	NC_50						
	205	GND_10	G		GND	GND		
	207	NC_51						
	209	NC_52						
	211	NC_53						
	213	NC_54						
	215	NC_55						
	217	NC_56						
	219	GND_11	G		GND	GND		
	221	PWRON			POWER_ON	Power on Signal Input, External connection Power key , active low		
	223	NC_57						
	225	VCC_IO_1	P		VCC_IO	Output Voltage 3.3V,Rated output current 300mA	3.3V	



接口定义 Interface definition

	227	VCC_IO_2	P		VCC_IO	Output Voltage 3.3V, Rated output current 300mA	3V	
	229	VCC_18_1	P		VCC_18	Output Voltage 1.8V, Rated output current 300mA	1.8V	
	231	NC_58						
	233	VCC_5V_S	P		VCC_5V_S	Input Voltage 5V, Rated input current 50mA (System startup power supply)	5V	
	235	VCC_IO_3	P		VCC_IO	Output Voltage 3.3V, Rated output current 300mA	3.3V	
	237	VCC_IO_4	P		VCC_IO		3.3V	
	239	VCC_IO_5	P		VCC_IO		3.3V	
	241	GND_12	G		GND	Power ground		
	243	GND_13	G		GND			
	245	GND_14	G		GND			
	247	GND_15	G		GND			
	249	GND_16	G		GND			
	251	VCC_SYS_1	P		VCC_SYS	System Power supply Input Voltage : Min 4.8V, Typ 5V, Max 5.2V Input current: Typ 450mA ;Max 950mA	5V	
	253	VCC_SYS_3	P		VCC_SYS		5V	
	255	VCC_SYS_5	P		VCC_SYS		5V	
	257	VCC_SYS_7	P		VCC_SYS		5V	
	259	VCC_SYS_9	P		VCC_SYS		5V	
Part B	pin	Core board pin definition	Pin type	I/O Pull	Default function	Default function description	IO Power domain	RK3328 Pin Number
	2	GND_17	G		GND	GND		
	4	GPIO2_C2/I2S1_SCLK/PDM_CLK_M0/TSP_D7_M1/CIF_D7_M1_D_3.3V	I/O	DOWN	GPIO2_C2_D/I2S1_SCLK	I2S serial clock	3.3V	R18



接口定义 Interface definition

	6	GPIO2_C0/I2S1_LRCK_RX/TSP_D5_M1/CIF_D5_M1_U_3.3V	I/O	UP	GPIO2_C0_U/I2S1_LRCK_RX	I2S serial data	3.3V	V15
	8	GPIO2_C1/I2S1_LRCK_TX/SPDIF_TX_M1/TSP_D6_M1/CIF_D6_M1_U_3.3V	I/O	UP	GPIO2_C1_U/I2S1_LRCK_TX	I2S serial data	3.3V	P18
	10	GPIO2_C3/I2S1_SDI/PDM_SDI0_M0/CARD_CLK_M1_U_3.3V	I/O	UP	GPIO2_C3_U/I2S1_SDI	I2S serial data input	3.3V	U16
	12	GPIO2_C7/I2S1_SDO/PDM_FSYNC_M0_U_3.3V	I/O	UP	GPIO2_C7_U/I2S1_SDO	I2S serial data output	3.3V	N17
	14	GPIO2_C6/I2S1_SDIO3/PDM_SDI3_M0/CARD_IO_M1_U_3.3V	I/O	UP	GPIO2_C6_U/I2S1_SDO3	Configurable I2S serial data output	3.3V	V16
	16	GPIO2_C5/I2S1_SDIO2/PDM_SDI2_M0/CARD_DET_M1_U_3.3V	I/O	UP	GPIO2_C5_U/I2S1_SDO2	Configurable I2S serial data output	3.3V	V17
	18	GPIO2_C4/I2S1_SDIO1/PDM_SDI1_M0/CARD_RST_M1_U_3.3V	I/O	UP	GPIO2_C4_U/I2S1_SDO1	Configurable I2S serial data output	3.3V	V18
	20	GPIO2_B7/I2S1_MCLK/TSP_SYNC_M1/CIF_CLKOUT_M1_D_3.3V	I/O	DOWN	GPIO2_B7_D/I2S1_MCLK	I2S clock source	3.3V	N18
	22	GPIO2_A4/PWM0/I2C1_SDA_3.3V	I/O	UP	I2C1_SDA_PMIC	I2C serial port 3,for PMIC , Core board interiorl pull up Resistor 2.2K	3.3V	N19
	24	GPIO2_A5/PWM1/I2C1_SCL_3.3V	I/O	UP	I2C1_SCL_PMIC	I2C serial port 3,for PMIC , Core board interiorl pull up Resistor 2.2K	3.3V	N20
	26	GND_18	G		GND	GND		
	28	GPIO_MUTE_D_3.3V			SPK_MUTE	Speaker silence function	3.3V	N2
	30	NC_59						
	32	NC_60						
	34	NC_61						
	36	NC_62						
	38	NC_63			GND/NC	GND/NC(Pull down 10K to the ground)	GND/NC	
	40	GND_19	G		GND	GND		
	42	GPIO3_B0/TSP_D4/CIF_D4/SPI_CSN0_M2/I2S2_LRCK_TX_M1/USB3PHY_D EBUG8/I2S2_LRCK_RX_M1_D_3.3V	I/O	DOWN	WIFI_REG_ON_H	WIFI module power enable 1:Enable 0:Disable	3.3V	F3



接口定义 Interface definition

	44	GPIO3_A1/TSP_FAIL/CIF_HREF/SDMMC0EXT_DET/SPI_TXD_M2/USB3PHY_DEBUG2/I2S2_SDO_M1_U_3.3V	I/O	UP	WIFI_WAKE_HOST	WIFI module wake up AP	3.3V	D2
	46	GPIO3_A6/TSP_D2/CIF_D2/SDMMC0EXT_D2/UART1_RX/USB3PHY_DEBUG6_U_3.3V	I/O	UP	SDIO0_D2	SDIO0 data port , for WIFI module	3.3V	F2
	48	GPIO3_A7/TSP_D3/CIF_D3/SDMMC0EXT_D3/UART1_CTSN/USB3PHY_DEBUG7_U_3.3V	I/O	UP	SDIO0_D3	SDIO0 data port , for WIFI module	3.3V	F1
	50	GPIO3_A0/TSP_VALID/CIF_VSYNC/SDMMC0EXT_CMD/SPI_CLK_M2/USB3PHY_DEBUG1/I2S2_SCLK_M1_U_3.3V	I/O	UP	SDIO0_CMD	SDIO0 command output , for WIFI module	3.3V	E3
	52	GPIO3_A2/TSP_CLK/CIF_CLKIN/SDMMC0EXT_CLK/SPI_RXD_M2/USB3PHY_DEBUG3/I2S2_SDI_M1_D_3.3V	I/O	DOWN	SDIO0_CLK	SDIO0 clock output, for WIFI module	3.3V	E1
	54	GPIO3_A4/TSP_D0/CIF_D0/SDMMC0EXT_D0/UART1_TX/USB3PHY_DEBUG4_U_3.3V	I/O	UP	SDIO0_D0	SDIO0 data port , for WIFI module	3.3V	E2
	56	GPIO3_A5/TSP_D1/CIF_D1/SDMMC0EXT_D1/UART1_RTSN/USB3PHY_DEBUG5_U_3.3V	I/O	UP	SDIO0_D1	SDIO0 data port , for WIFI module	3.3V	D1
	58	GND_20	G		GND	GND		
	60	RK805_32KOUT_3.3V			RK805_32KOUT	Output 32.768K CLK	3.3V	
	62	NC_64						
	64	NC_65						
	66	NC_66						
	68	NC_67						
	70	NC_68						
	72	VCC_18	P		1.8V	1.8V (no used)	1.8V	
	74	GPIO1_D2/I2S2_LRCK_RX_M0/CLKOUT_GMAC_M2/PDM_SDI3_M1_D_3.3V	I/O	DOWN	BT_WAKE_HOST	BT module wake up AP	3.3V	V12
	76	NC_69						
	78	NC_70						
	80	NC_71						
	82	GPIO1_D4/CLK32KOUT_M1_D_3.3V	I/O	DOWN	MIPI_CSI_D2P	MIPI-DSI0 differential lane 2 positive	3.3V	V14



接口定义 Interface definition

	84	NC_72						
	86	NC_73						
	88	NC_74						
	90	NC_75						
	92	NC_76						
	94	NC_77						
	96	NC_78						
	98	GPIO0_D6/FEPHY_LED_SPEED10/SDMMC0_PWREN_M1_D_3.3V	I/O	DOWN	HP_DET	Headphone detection	3.3V	W10
	100	GPIO2_A1/UART2_RX_M1/POWERSTATE1_U_3.3V	I/O	UP	UART2_RX	Uart2 serial port data input, for AP debug	3.3V	P20
	102	GPIO2_A0/UART2_TX_M1/POWERSTATE0_D_3.3V	I/O	DOWN	UART2_TX	Uart2 serial port data output ,for AP debug	3.3V	P19
	104	NC_79						
	106	GPIO2_A2/IR_RX/POWERSTATE2_U_3.3V	I/O	UP	IR_IN/UART3_RX/GPIO0_C1	IR receiver input	3.3V	M21
	108	NC_80						
	110	NC_81						
	112	GND_21	G		GND	GND		
	114	NC_82						
	116	NC_83						
	118	NC_84						
	120	NC_85						
	122	VDAC_IOUT	O		VDAC_IOUT	Positive output (no used)		M2



接口定义 Interface definition

	124	NC_86						
	126	NC_87						
	128	NC_88						
	130	NC_89						
	132	GND_22	G		GND	GND		
	134	NC_90						
	136	NC_91						
	138	NC_92						
	140	NC_93						
	142	NC_94						
	144	NC_95						
	146	NC_96						
	148	NC_97						
	150	SARADC_IN1			SARADC_IN1	ADC input , Core board interiorl pull up Resistor 10K	1.8V	M17
	152	SARADC_IN0			RECOVER	AD keyboard input , Core board interiorl pull up Resistor 10K	1.8V	M18
	154	NC_98						
	156	NC_99						
	158	NC_100						
	160	NC_101						
	162	NC_102						



接口定义 Interface definition

	164	NC_103						
	166	NC_104						
	168	NC_105						
	170	NC_106						
	172	NC_107						
	174	NC_108						
	176	NC_109						
	178	NC_110						
	180	GND_23	G		GND	GND		
	182	GPIO1_C3/SDMMC1_DET/GMAC_MDIO_M1/PDM_FSYNC_M1_U_3.3V	I/O	UP	RMII_MDIO	MAC management interface data	3.3V	Y21
	184	GPIO1_C7/I2S2_LRCK_TX_M0/GMAC_MDC_M1/PDM_SDI0_M1_D_3.3V	I/O	DOWN	MDC_MAC	MAC management clock	3.3V	W17
	186	GPIO1_B4/SDMMC1_CLK/GMAC_TXCLK_M1_D_3.3V	I/O	DOWN	PHY_TXCLK	PHY_TXCLK , Core board internal series resistance 22R (no used)	3.3V	AA20
	188	GPIO1_B5/SDMMC1_CMD/GMAC_RXCLK_M1_U_3.3V	I/O	UP	RMII_RXER	MAC RX error signal	3.3V	Y20
	190	GND_24	G		GND	GND		
	192	GPIO1_C5/I2S2_MCLK/GMAC_CLK_M1_D_3.3V	I/O	DOWN	RMII_CLK	MAC REC_CLK output or external clock input	3.3V	W15
	194	GPIO1_B2/UART0_RTSN/GMAC_RXD1_M1_D_3.3V	I/O	DOWN	RMII_RXD1	MAC RX data	3.3V	W14
	196	GPIO1_B6/SDMMC1_D0/GMAC_RXD3_M1_U_3.3V	I/O	UP	MAC_RXD3	MAC RX data (no used)	3.3V	W19
	198	GPIO1_B3/UART0_CTSN/GMAC_RXD0_M1_D_3.3V	I/O	DOWN	RMII_RXD0	MAC RX data	3.3V	V13
	200	GPIO1_B7/SDMMC1_D1/GMAC_RXD2_M1_U_3.3V	I/O	UP	MAC_RXD2	MAC RX data (no used)	3.3V	W18



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	202	GPIO1_C6/I2S2_SCLK_M0/GMAC_RXDV_M1/PDM_CLK_M1_U_3.3V	I/O	UP	RMII_RXDV	MAC RX enable 1:Enable 0:Disable	3.3V	W16
	204	GPIO1_B1/UART0_TX/GMAC_TXD0_M1_U_3.3V	I/O	UP	RMII_TXD0	MAC TX data , Core board interiorI pull up Resistor 4.7K	3.3V	AA15
	206	GPIO1_C1/SDMMC1_D3/GMAC_TXD2_M1_U_3.3V	I/O	UP	PHY_TXD2	MAC TX data , Core board interiorI pull up Resistor 4.7K (no used)	3.3V	Y19
	208	GPIO1_C0/SDMMC1_D2/GMAC_TXD3_M1_U_3.3V	I/O	UP	PHY_TXD3	MAC TX data , Core board interiorI pull up Resistor 4.7K (no used)	3.3V	AA19
	210	GPIO1_B0/UART0_RX/GMAC_TXD1_M1_U_3.3V	I/O	UP	RMII_TXD1	MAC TX data , Core board interiorI pull up Resistor 4.7K	3.3V	Y15
	212	GPIO1_D1/I2S2_SDO_M0/GMAC_TXEN_M1/PDM_SDI2_M1_D_3.3V	I/O	DOWN	RMII_TXEN	MAC TX data enable , Core board internal series resistance 22R 1:Enable 0:Disable	3.3V	Y17
	214	NC_111						
	216	GPIO1_C2/SDMMC1_PWREN/GMAC_CRD_M1_D_3.3V	I/O	DOWN	RMII_RST	MAC reset	3.3V	W20
	218	NPOR_U_3.3V	I		RESET_KEY	system reset signal Input,External connection Reset key,active low , Core board interiorI pull up Resistor 10K	3.3V	P21
	220	POWER_EN			EXT_EN	External Power enable output,Voltage 5V 1:Enable 0:Disable	5V	
	222	NC_112						
	224	GND_25	G		GND	GND		
	226	VCC_IO_6	P		VCC_IO	Output Voltage 3.3V,Rated output current 300mA	3.3V	
	228	VCC_18_2	P		VCC_18	Output Voltage 1.8V,Rated output current 300mA	1.8V	
	230	NC_113						
	232	VCC_RTC	P		VCC_RTC	Input Voltage 5V, Rated input current 50mA (Systemstartup power supply)	3.3V/5.0V In	
	234	VCC_IO_7	P		VCC_IO	Output Voltage 3.3V,Rated output current 300mA	3.3V	
	236	NC_114						



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	238	VCC_IO_8	P		VCC_IO	Output Voltage 3.3V, Rated output current 300mA	3.3V	
	240	GND_26	G		GND	Power ground		
	242	GND_27	G		GND			
	244	GND_28	G		GND			
	246	GND_29	G		GND			
	248	GND_30	G		GND			
	250	GND_31	G		GND			
	252	VCC_SYS_2	P		VCC_SYS	System Power supply Input Voltag : Min 4.8V, Typ 5V, Max 5.2V Input current: Typ 450mA ;Max 950mA	5.0V	
	254	VCC_SYS_4	P		VCC_SYS		5.0V	
	256	VCC_SYS_6	P		VCC_SYS		5.0V	
	258	VCC_SYS_8	P		VCC_SYS		5.0V	
	260	VCC_SYS_10	P		VCC_SYS		5.0V	
	261	GND_32	G		GND	Power ground		
	262	GND_33	G		GND			
	263	GND_34	G		GND			
	264	GND_35	G		GND			
	265	GND_36	G		GND			
	266	GND_37	G		GND			



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